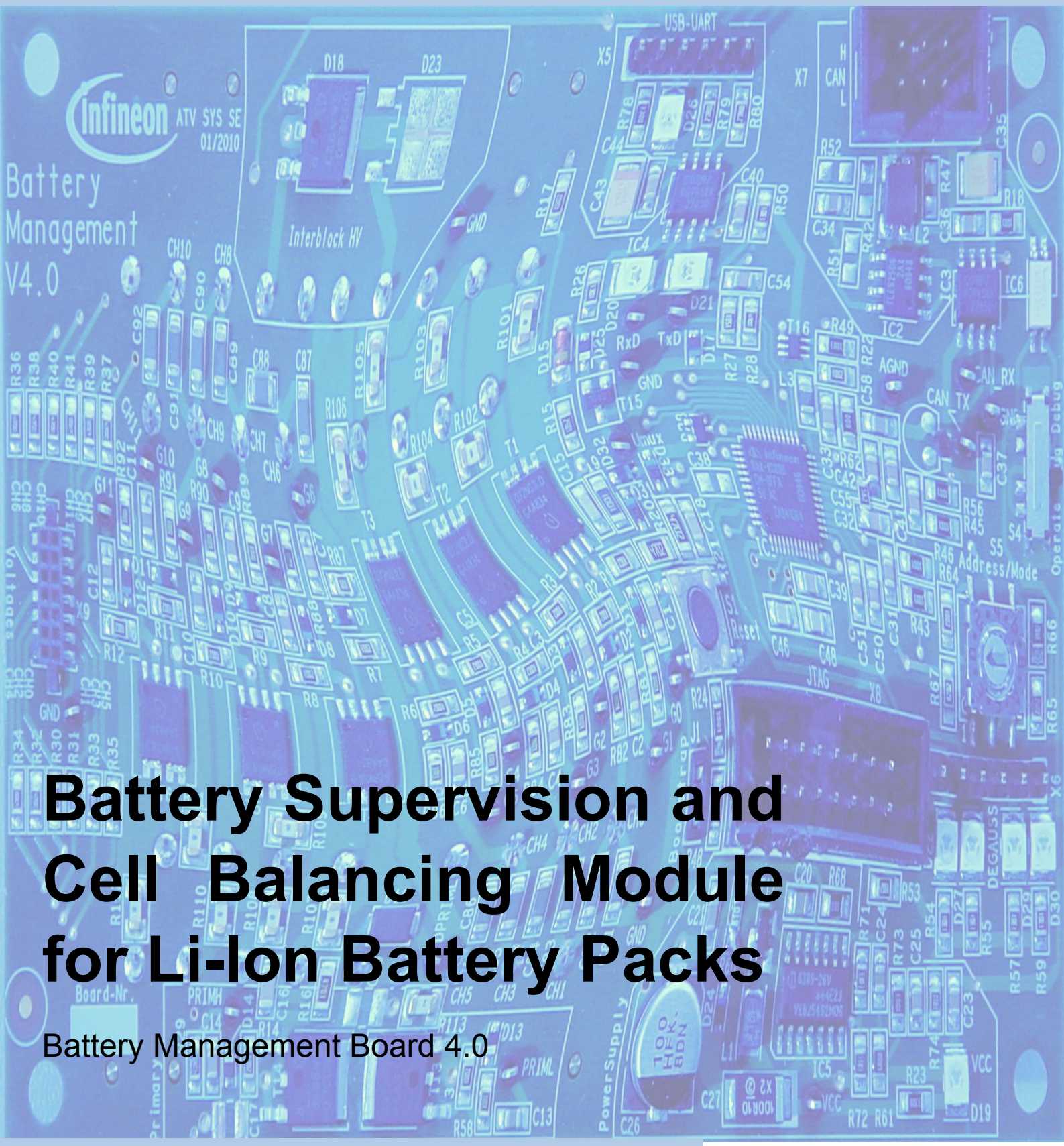
Rev 1.3 ; 2010-06-24



Battery Supervision and Cell Balancing Module for Li-Ion Battery Packs

Battery Management Board 4.0

System Engineering Automotive

Never stop thinking

Edition 2010-06-24

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Battery Mangagement Module Battery Supervision and Cell Balancing Module for Li-Ion Packs

Revision History: 2010-06-24, Rev 1.3

New in Version: 1.1	
Page 17	New Paragraph: Degauss Monitoring
New in Version: 1.2	
Page 25	New Paragraph: “Wiring Example of a Battery Block
New in Version: 1.21	
Page 35	Part number for fuses in BOM
Page 31	New Paragraph: Pulse Sequences (Screenshots)
New in Version: 1.3	
Page 32	New Paragraph: Initial Test and Calibration Procedure

1 Introduction

The board version 4.0 is an evolution of the older version 3.1. The main intention of the development was the target of a safer operation even under extreme conditions.

Improvements compared to version 3.1

- Switching regulator for V_{CC} generation *(IC5)*
  - Wider operation range
  - Highest efficiency
  - Symmetrical load for all cells
- New MOSFETs for secondary switches in dual Super SO8 packages *(T1 to T6)*
  - Saving board space
  - Saving costs
- Fuses for all transformer windings *(R101 to R112)*
- Transformer degauss monitoring
- Potential free UART interface *(IC4)*
- Noise filter for CAN lines (*L2*)
- Additional LEDs for status indication
- Reset button
- Jumper for bootstrap mode (*J1*)
- Diagnosis connector for calibration *(X9)*
- Additional test points

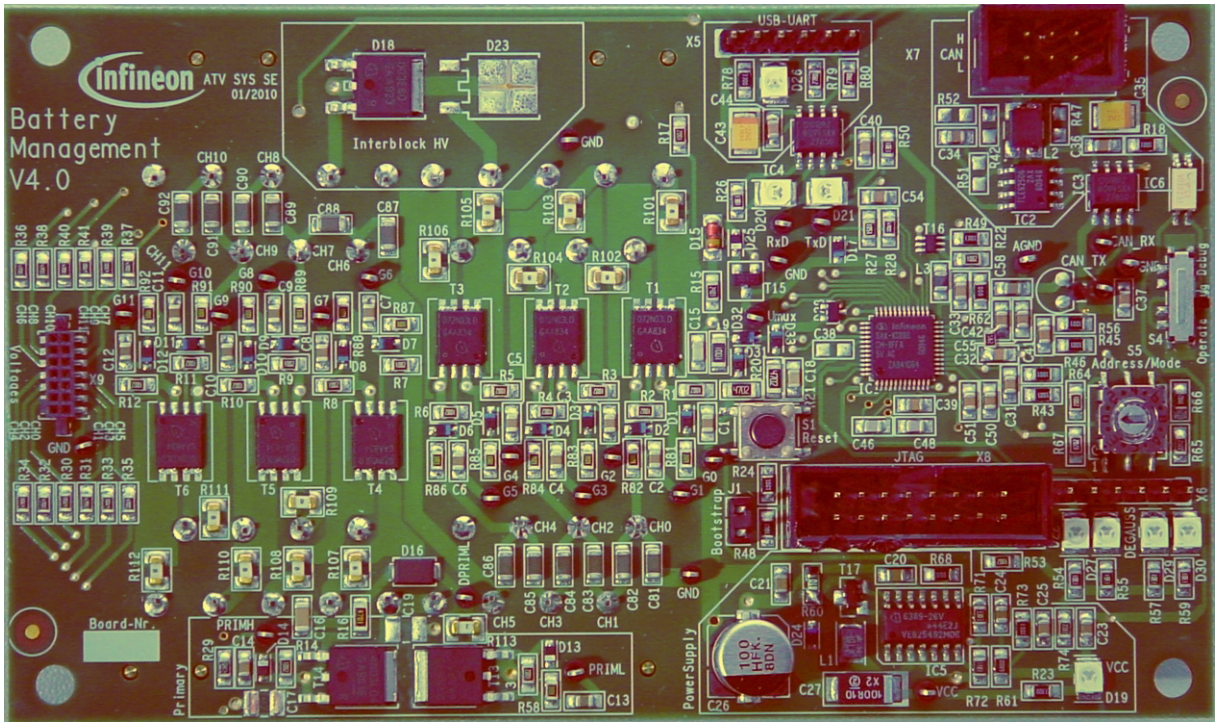

Figure 1 Board Photo

2 Circuit Description

2.1 Power Supply

For the generation of the supply voltage V_{CC}, a step-down converter is used. This allows a highest efficiency over a wide input voltage range. The integrated voltage regulator TLE6389-2GV is used to control the switch BSS83P.

The input is connected to the CH11 voltage, which represents the complete block voltage. Therefore all cells are burdened with the same load.

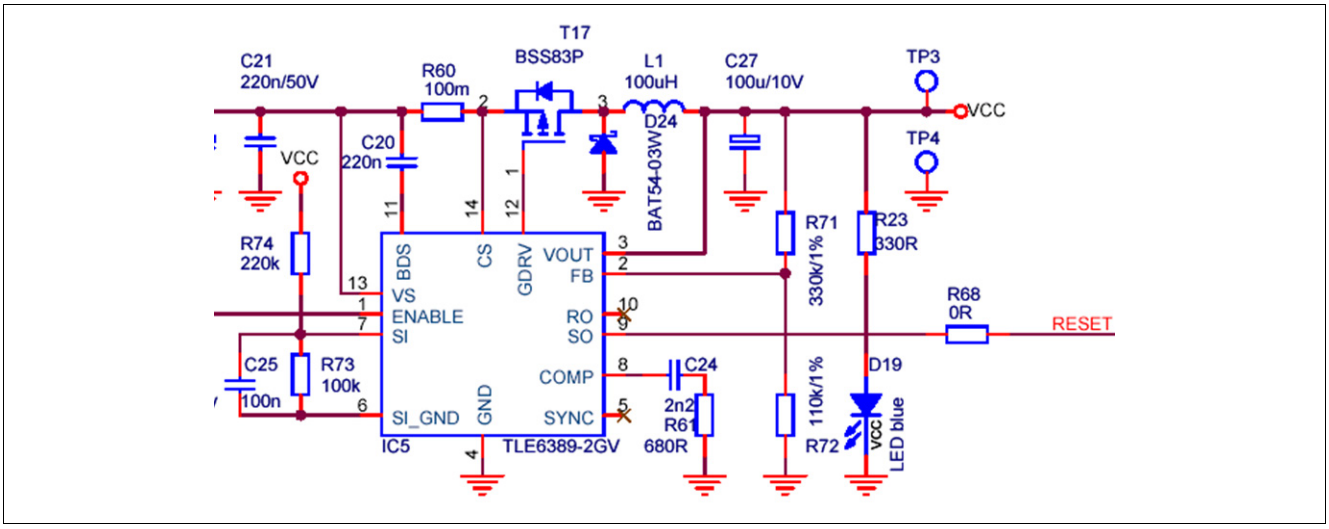

Figure 2 Voltage regulator

The blue LED D19 indicates the presence of V_{CC}.

2.1.1 Under voltage Protection

With the voltage divider R74/R73, the output voltage V_{CC} is monitored. If it is too low, a reset for the µC is generated.

2.1.2 Interlock and On/Off Switch

The interlock loop ensures, that the board only works, if it is plugged correctly.

It is dangerous, when the µController activates any MOSFETs, when not all cells are connected properly.

The V_{CC} supply voltage is only available, if following conditions are fulfilled:

- X2, X3 and X4 are plugged
- S4 is in position 'debug'
  or S4 in position 'operate' **and** the opto coupler IC6 is active

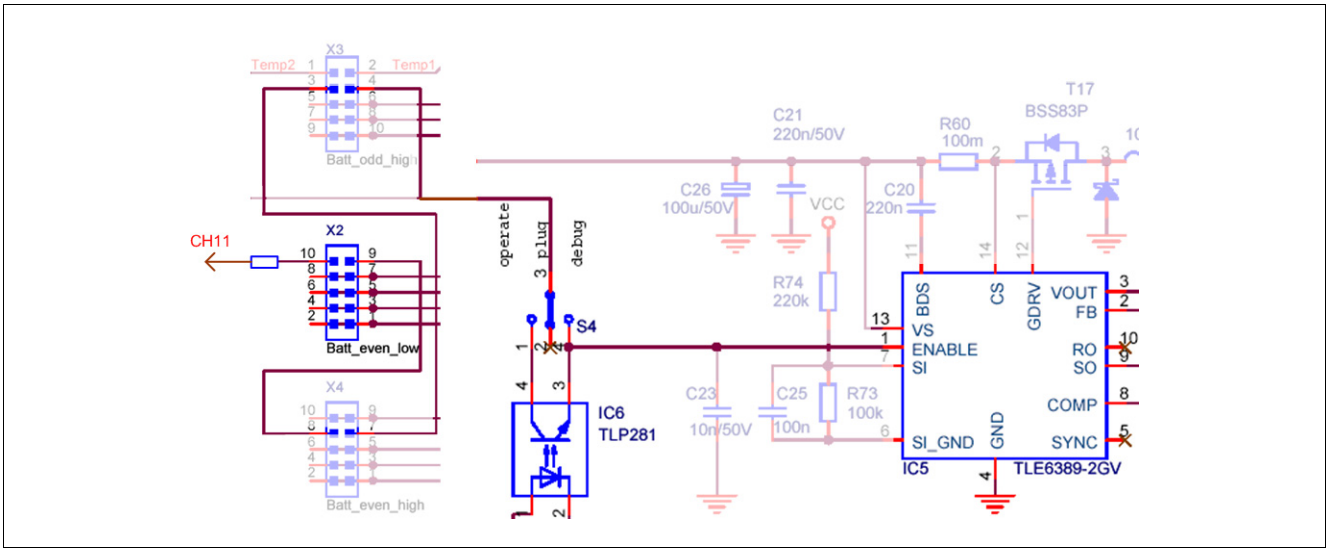

Figure 3 Interlock Loop

2.1.3 Sleep Mode

The complete battery block V_{CC} can be switched off over the opto coupler IC6.

Note: The opto coupler is only in the loop, if S4 is in the position 'operate'.

2.1.4 Power Supply Operation Control

When the battery block is not in operation, the control circuit should not be powered. This avoids a needless self discharge. The voltage regulator consumes about 2µA in the off mode (V_{EN}= 0V).

Depending on the use of the board, two different operation modes are possible.

They are selected with the switch S4.

- **Debug Mode**
  The V_{CC} voltage is always available, when the 'Connect' signal is present.
  In this mode, the Mode switch S3 is usually in position '0'.
- **Operate Mode**
  The V_{CC} voltage can be remotely switched on over the opto coupler IC9 from the battery system master.

2.2 Temperature Measurement

The temperature is measured at four different locations. One temperature sensor is placed on the PCB, three others have to be distributed between the battery cells.

The battery sensors are linked over the connectors X1 and X3.

It is important to monitor the battery temperature in order to get a good battery lifetime. Simple voltage dividers of a KTY type silicon temperature sensor and a resistor produce a temperature dependent voltage to a ADC inputs of the µController.

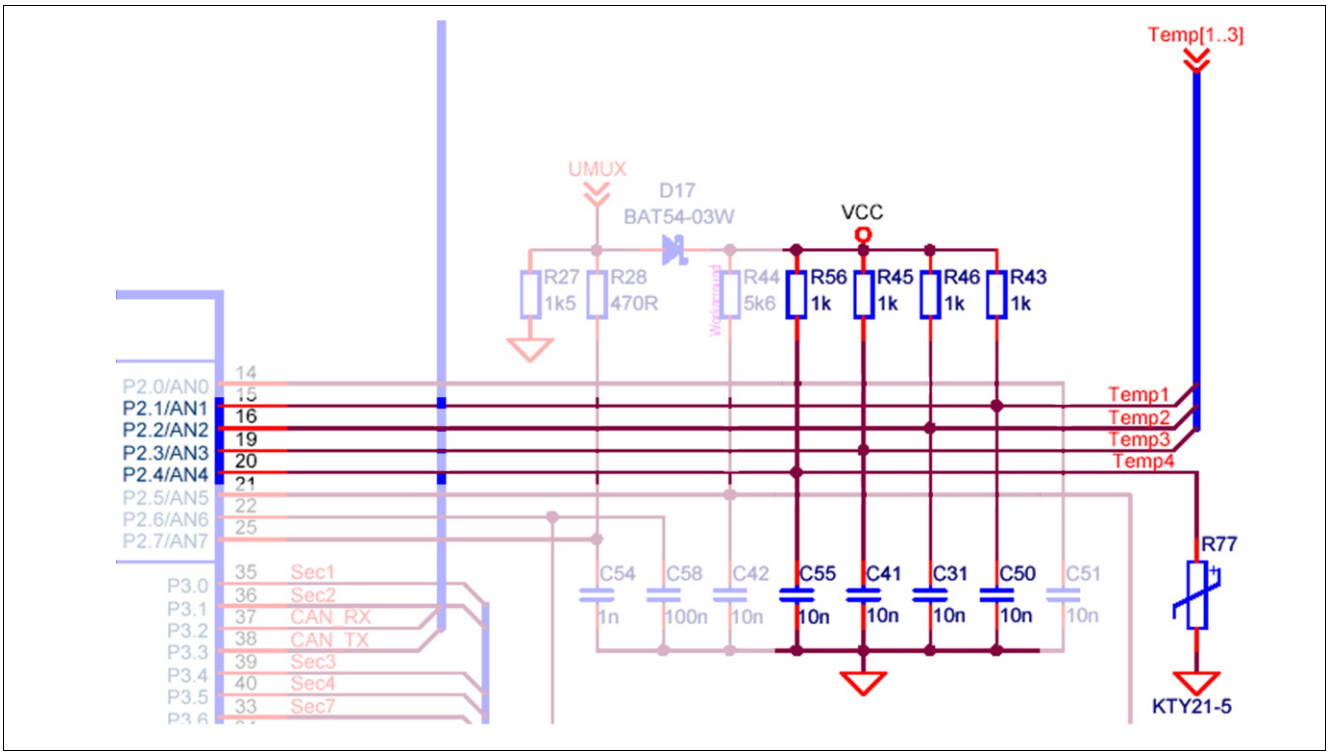

Figure 4 Temperature Measurement

2.3 Mode Switch

The rotary mode switch has 16 positions. In each of these positions, a different DC voltage can be measured at the AN5 input.

- Mode 0: Test mode for control via terminal software
- Mode_ 1 to 15: Slave address

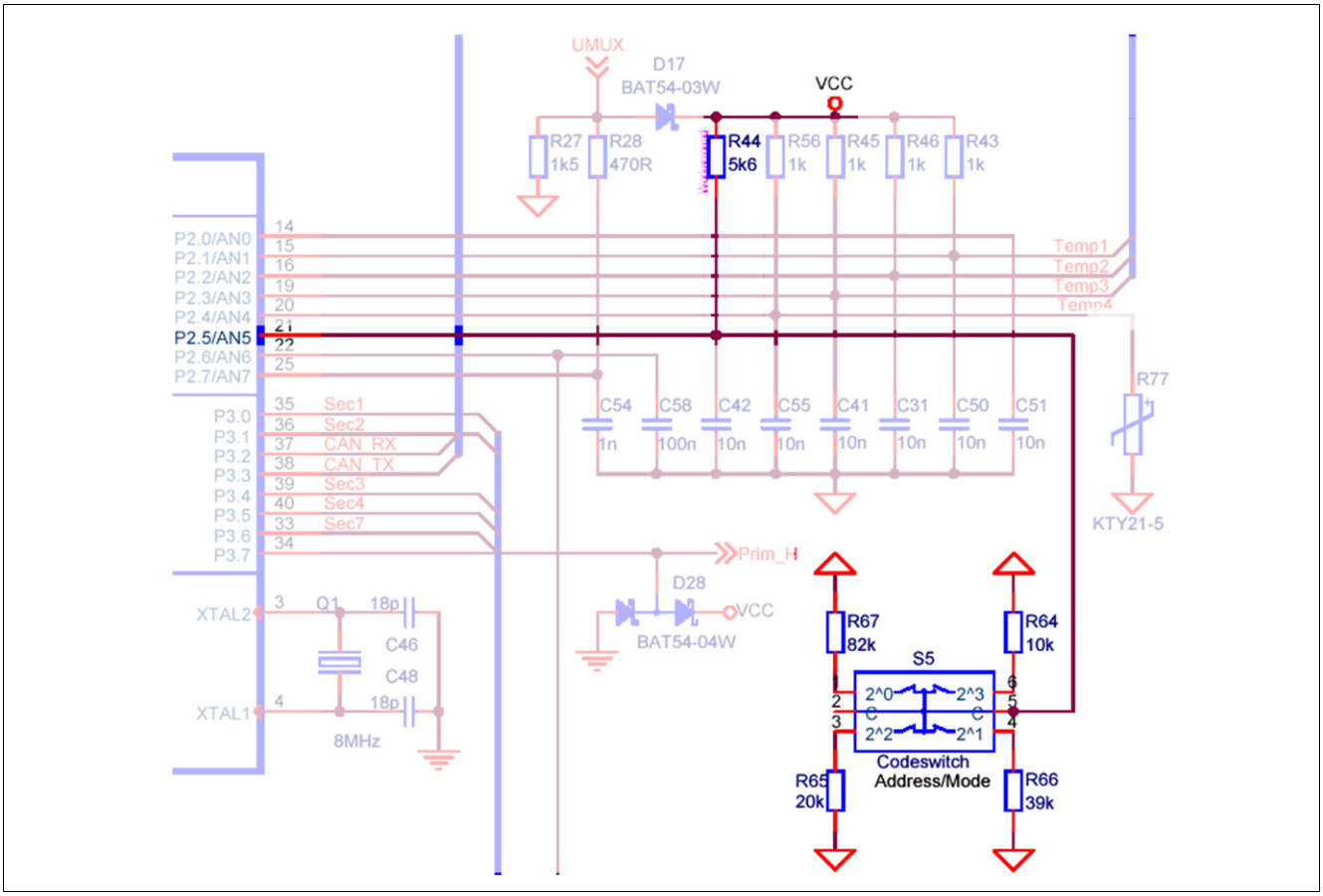

Figure 5 Mode Switch

2.4 Communication Interfaces

2.4.1 CAN

As every slave board is at a different potential, they have to be isolated from each other. Only the master board is related to the vehicle ground potential.

An isolated CAN port allows the communication between a system master and the slaves. The ADUM1201 is a coreless transformer for data transmission. The conversion of the serial signal RX and TX into CAN signal is done by the integrated CAN interface TLE6250.

The isolated side of the ADUM (pins 5 to 8) and the TLE6250 are powered from the master board.

Pin 3 of the connector X7 supplies 5V and pin 4 is the Ground.

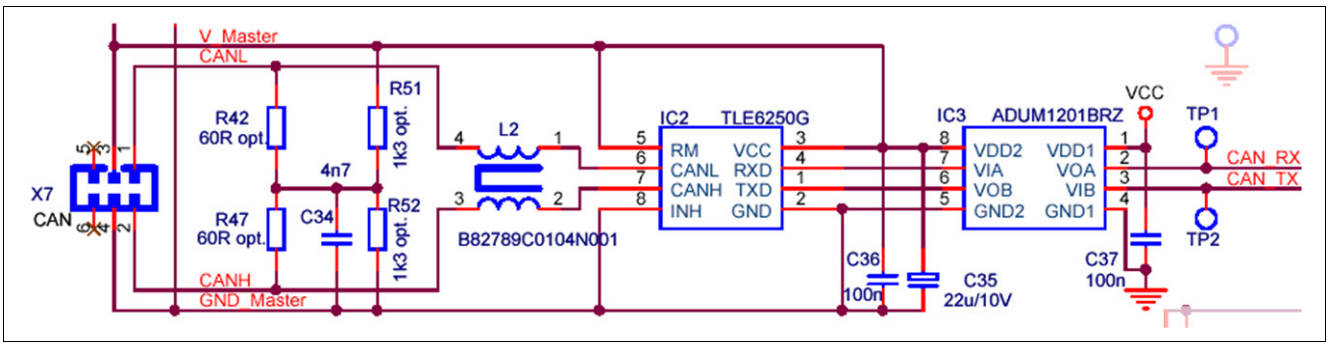

Figure 6 Isolated CAN Interface

2.4.2 Debugging Facilities

2.4.2.1 JTAG Debugging Interface

The connector X8 provides all signals for the link to a comfortable JTAG debugging interface.

It can be used for

- Software development
- Program flashing of the µController

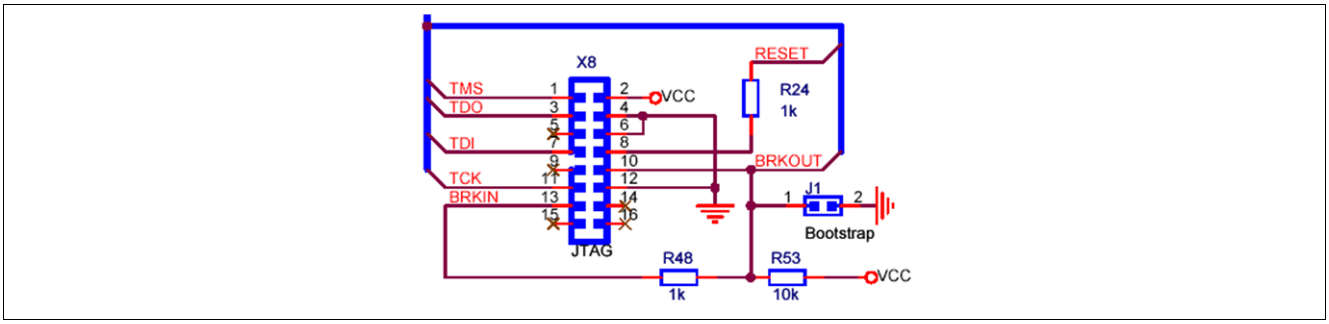

Figure 7 JTAG Debugging Connector

Software Update

The software in the µController Flash memory can be updated without a debugger environment. In this case, the µController has tom be booted in the ‘Bootstrap’ mode.

Note: The jumper J1 has to be plugged to bring the µController into the ’Bootstrap’ mode. The procedure for a software update is described in *“Software Update” on Page 11**.*

2.4.2.2 Diagnosis and Calibration Connector

Connector X9 can be used for the measurement of all cell voltages. The resistors in series avoid high currents in case of external short circuits.

For a comfortable calibration of the boards it is useful to prepare a connector to a multi-input voltmeter. An example is the ‘Integra 2700’ of Keithley.

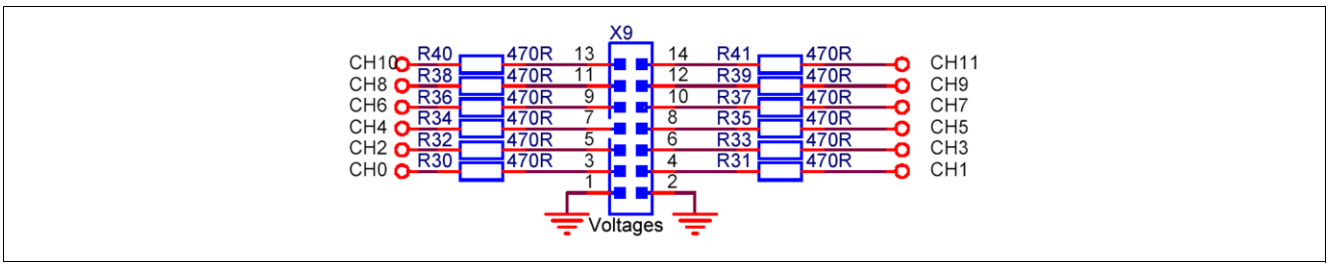

Figure 8 Voltage Measurement Connector

A suitable connector: Samtec TFSD-07-28-H-10.00-S.

2.4.2.3 Serial Connector and LED Indicators

Connector X9 is intended for the connection of a serial interface. With a serial - to RS232 or a serial - to USB interface, the communication with a PC is possible. During normal operation, permanent status messages are printed out for monitoring the status.

The connector pins fit directly to the USB interface cable available in the ‘Farnell’ catalogue (order #1329311).

The ADUM device is used as potential coupler for a potential free connection to a PC.

Communication Status LED

The LEDs allow a fast status visualization.

- D26 (red) is always on, when the isolated side of the ADUM is powered out of the interface. The voltage drop over the LED is used to reduce the incoming 5V to the 3.3V power supply of the ADUM device.
- D20 (green) shows RX activity at port P1.0
- D21 (yellow) shows TX activity at port P1.1

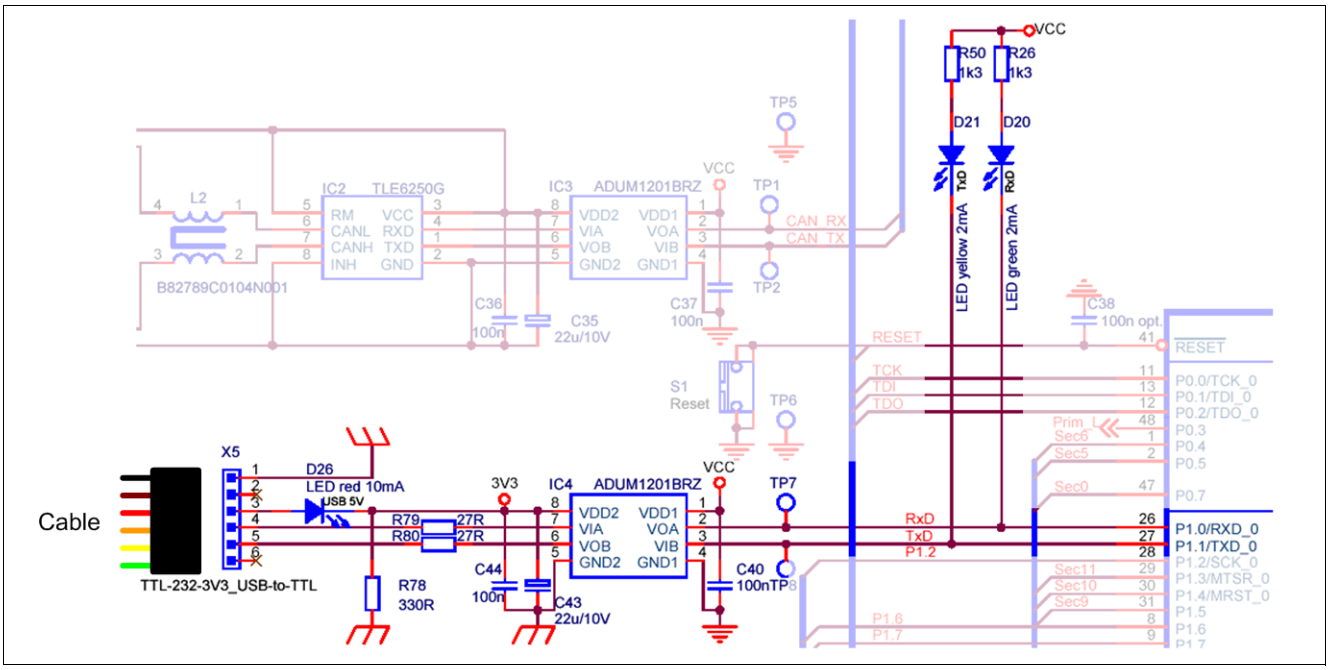

Figure 9 LED and serial Debugging Connector

2.4.2.4 Software Update

With the 'XC800_FLOAD' tool, a flash software update is possible.

Note: For a software update, the µController has to be in the bootstrap mode. During reset, the MBC pin has to be pulled down to GND (jumper J1 plugged).

Software Update Procedure:

1. Download the *FLOAD* tool from http://www.infineon.com/cms/en/product/channel.html?channel=db3a304319c6f18c011a0b54923431e5
2. In case of a missing DLL: Install the *Device Access Server* (DAS) from http://www.infineon.com/cms/en/product/promopages/das/ .
3. Plug a jumper at the J1 pins to prepare the bootstrap mode
4. Switch the V_{CC} off and on using S4 or press the Reset button
5. Connect X5 over a serial-to-RS232 or USB interface to a COM port
6. Start FLOAD.EXE
7. Select the µController type 'XC88x-8FF'
8. Load the new HEX file with the button 'Open File'
9. Press the button 'Download'
10. After a successful download press 'Disconnect' to release the COM port
11. Start a terminal software
12. Switch the V_{CC} off and on using S4 or press the Reset button.
13. The welcome message should show the new compilation date

2.5 Voltage Measurement

2.5.1 Block Voltage Measurement

The complete block voltage can be measured directly via the ADC input port AN6.

The voltage is divided with R39 and R22 to adapt it to the ADC input range.

The NPN/PNP combination T16A and T16B switches the voltage divider only on, when V_{CC} is present. So there is no current consumption in off mode.

The two complementary transistors T16A and T16B (BCR22PN) are placed together with the base resistors in a tiny SOT363 package.

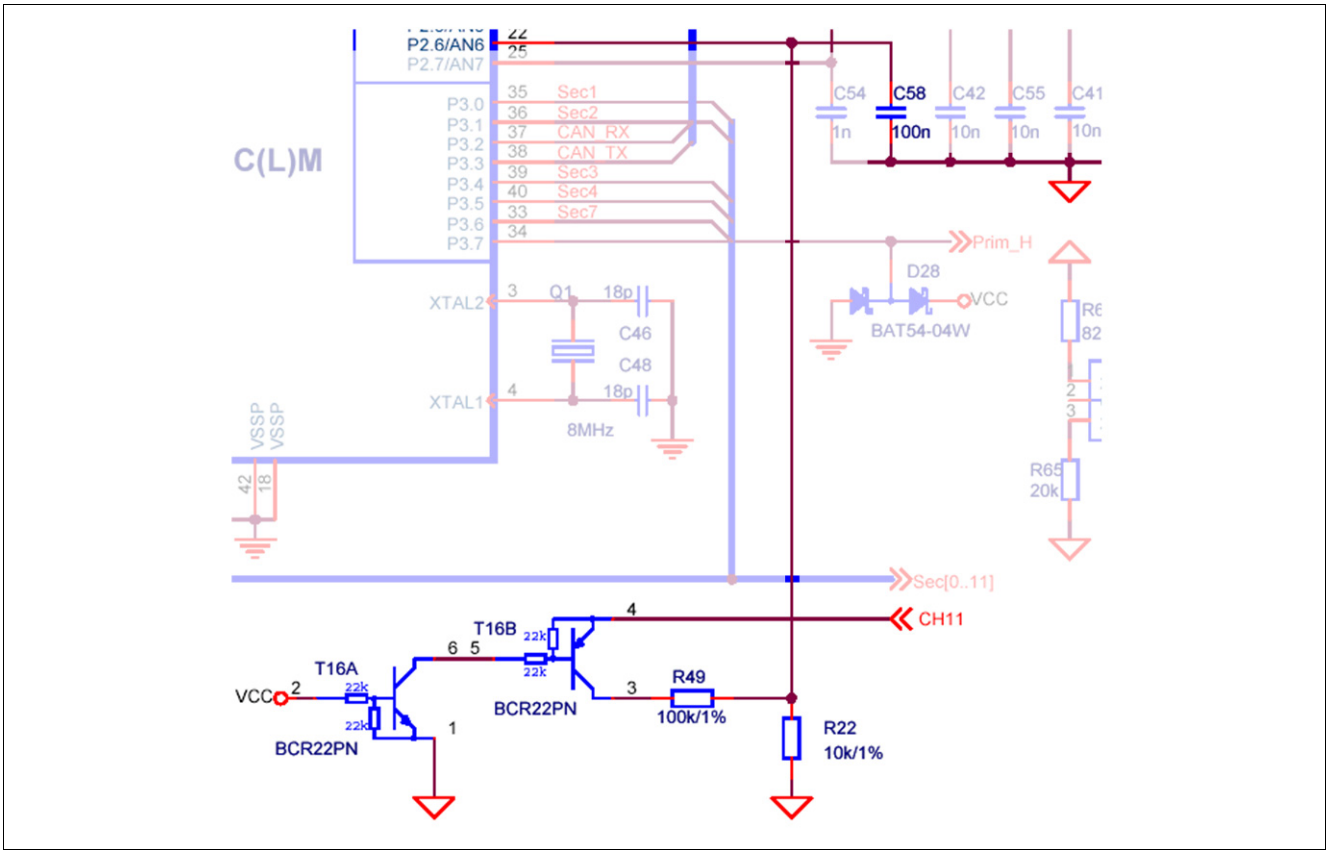

Figure 10 Block Voltage Measurement

2.5.2 Cell Voltage Measurement

Every cell is at a different potential, while the ADC input is near the block ground level. To connect the cell voltages to a common ADC input, a multiplexer as well as a level shifter is required. For both tasks the transformer is used.

Whenever one of the sec transistors is switched on, the corresponding cell voltage is available at all windings of the transformer. For the measurement path, the primary winding is used. This terminal is a common point for all cell voltages.

Caused by the winding direction, the measurement voltage at pin 8/11 is added to the block voltage U11. The value is also higher, as the primary winding has more turns.

The array R15, D15 and T15 is a current source, where the collector current out of T15 is proportional to the induced voltage in the primary winding.

$$I_C = \frac{U_{prim} - U_{D15} - U_{D25} - U_{BE}}{R15}$$

The voltage drops of D15, D25 and the Base-Emitter voltage of T15 are constant. This leads to an offset for the measurement voltage. The offset suppresses values below 2V cell voltage. As consequence only the 'interesting' range between 2V and 4.2V is projected to the ADC input range. So the 10 bit resolution is used most efficiently.

The current out of T15 is converted back into a ground related voltage in the resistor R27. The protection diode D17 limits the ADC input voltage to V_{CC} in case of overshootings. The RC combination R28 and the tank capacitor C54 works as low pass filter.

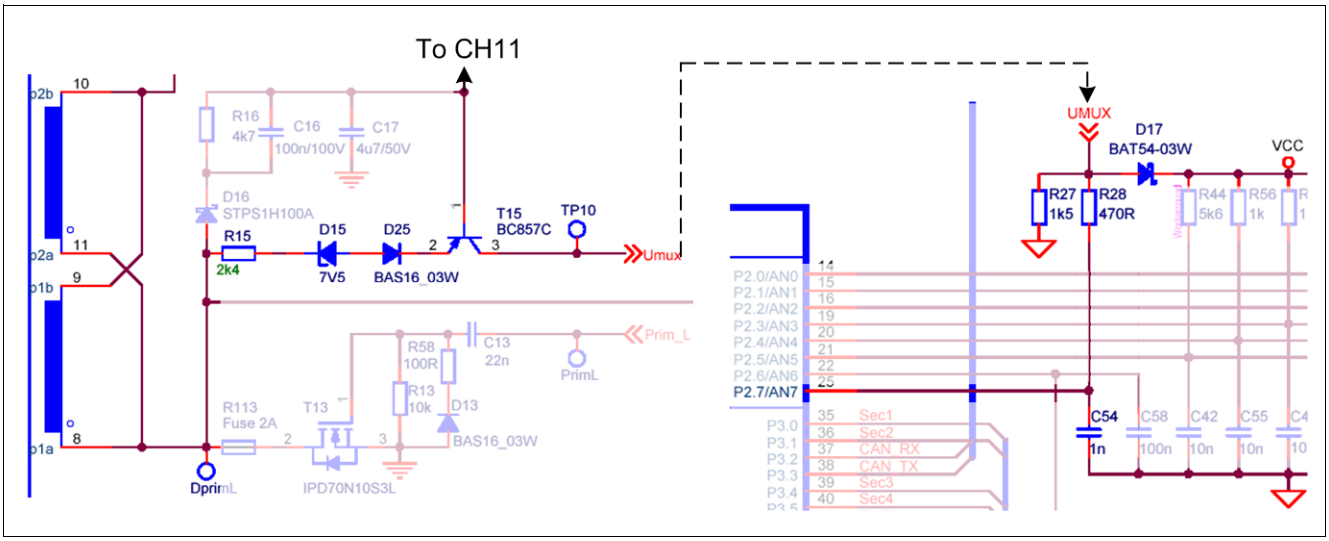

Figure 11 Cell Voltage Scan Circuit

Component Values for different Board Versions

Depending on the type of cells, the measurement path has to be adapted as follows. This tuning adapts the sensitivity and the offset to the operational voltage range.

The corresponding ADC values span from 0 to 1023.

Version	R15	D15	Range	Remarks
Normal Li-Ion cell	2k4	7V5	2.2V - 4.2V	Software for 12 cells
Nanosphosphate cell (A123)	2k0	7V5	2.1V - 3.7V	Software for 10 cells
Super Caps (Double Layer)	3k0	0 Ohm	0.3V - 2.8V	

2.6 Power Section

Heart of the power section is the transformer. It is used as energy storage element to move charge between the battery cells. As the principle is based on the flyback topology, the two sides are named ’primary’ and ’secondary’. The primary part is linked to the complete block voltage, the secondary parts to the individual cells.

2.6.1 Blocking Capacitor for Cell Voltages

The Capacitors C81 to C92 are parallel to the battery cells. They reduce the peak balancing currents in the connection wires to the cells.

The blocking capacitors reduce the influence of the parasitic ohmic and inductive resistance of the path from the transformer to the cells.

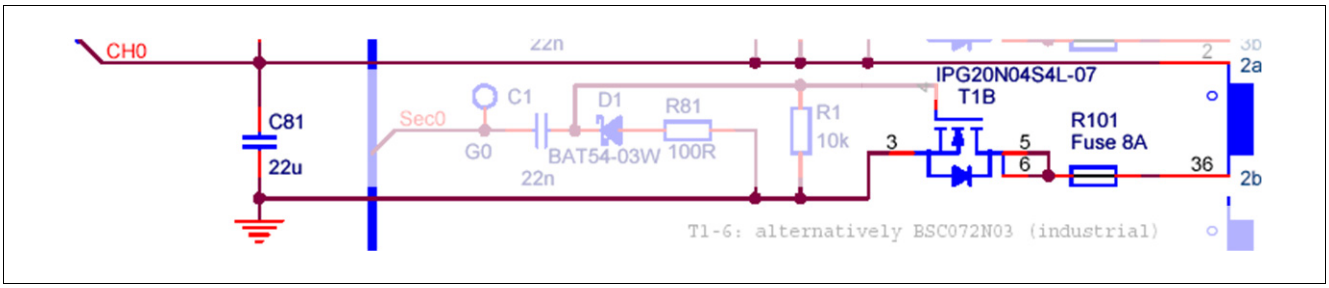

Figure 12 Blocking Capacitors

2.6.2 Fuses

The fuses in series to the transformer windings are for safety reasons. In case of a short circuit of the transistor, the current out of the battery cells is nearly unlimited. As consequence the PCB copper tracks would burn. The fuses blow before the PCB is damaged.

Usually such damages happen only in the development phase caused by handling errors.

The low resistance of 5mΩ minimizes the losses. The used fuse type is 451 from ‘Littelfuse’.

Note: For mass production the fuses can be skipped in order to save material cost and to improve the efficiency.

Note: In the schematics still the 8A value is shown. In later board versions it was increased to 10A. This reduces the losses and makes it less sensitive.

2.6.3 Secondary Switches

On the secondary side, every cell can be connected to a transformer winding over a MOSFET switch.

The figure below shows channel U1 as an example.

The LL (Logic Level) version of the MOSFETs IPG20N04S4L-08 allows to control them with the 5V output swing of the µController GPIO output directly.

The transistors T1 to T11 are switched on with a ’High’ pulse at the GPIO lines Sec0 to Sec11.

Like in the primary section, the time constant of C2 and R2 limits the pulse length.

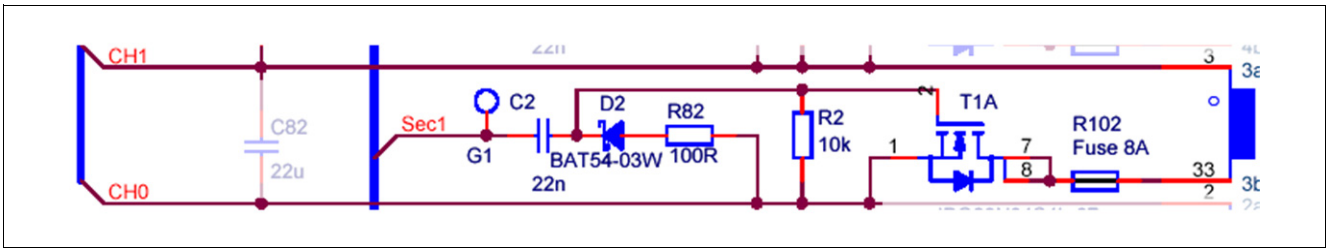

Figure 13 Secondary Channel

2.6.4 Primary Switch Circuitry

The primary side has two switches. One is located at ground level and represented by T13, a 100V MOSFET IPD70N10S3L. The high side of the winding is linked over T14 to U11. The high side transistor T14 is used to control the interblock balancing mode. As the blocking voltage is lower, a 30V type IPG20N04S4L-08 is used.

The transformer has two identical halves with the distributed secondary windings. For a better symmetrical coupling, each half has an identical primary winding. Both are connected in parallel.

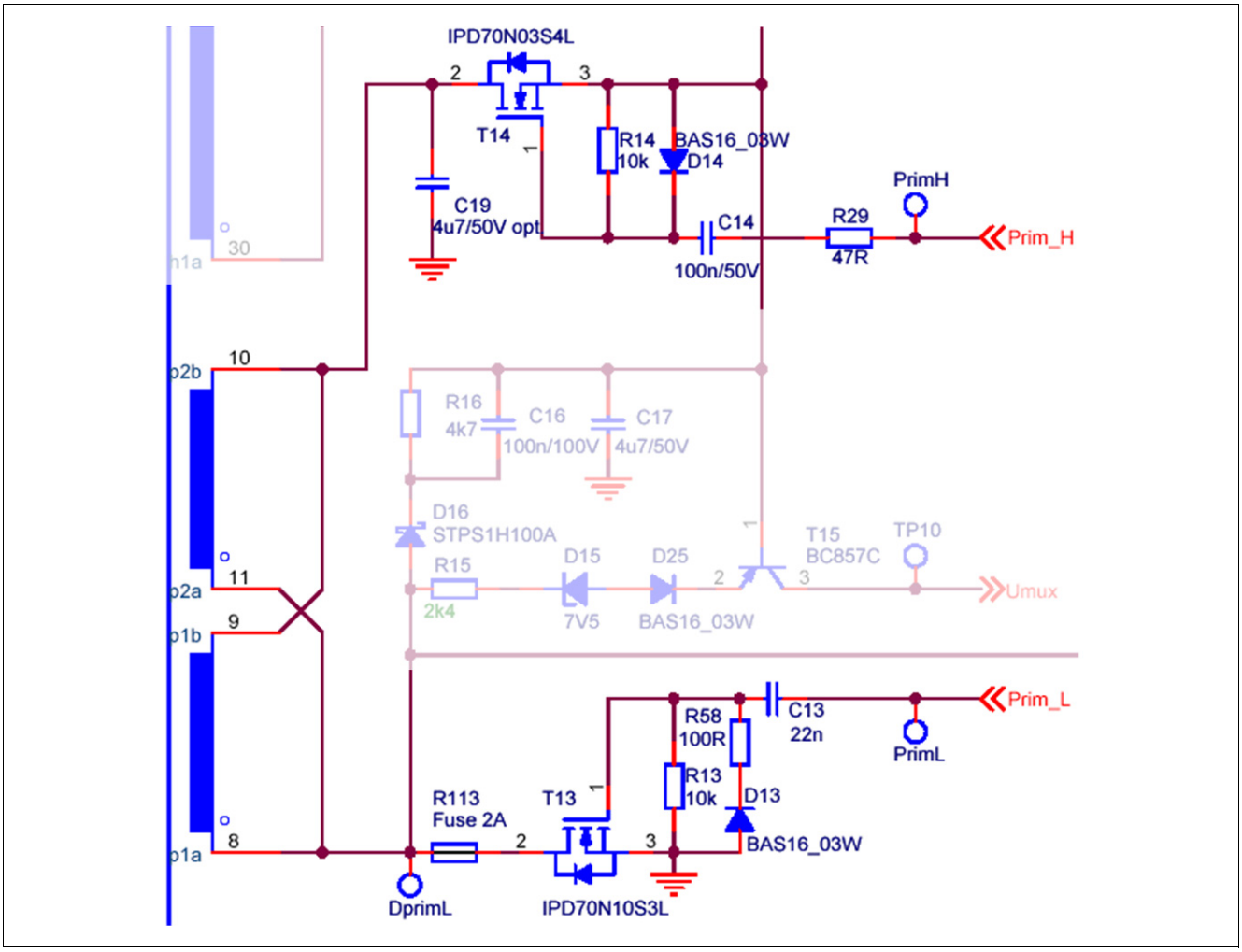

Figure 14 Primary Switch

Pulse Length Limitation

The board can be destroyed, if the transformer goes into saturation. As the current usually starts at zero, the value depends on

- Inductance
- Applied voltage
- On time

The high pass filter made of the resistor R13 and the capacitor C 13 limits the length of a positive gate pulse. This is only a prevention for the case that the µController delivers an erroneous permanent 'High' state on the GPIO output 'Prim'.

The high side transistor T14 works in series to T13. Therefore a longer on time is not critical.

2.6.5 Reduced Number of Cells

The board is designed with 12 channels to support the 12 battery cells of a block. This leads to lowest cost per channel.

If less channels (e.g.10) are used, following modifications are required:

- Replace any cells by a short circuit outside the board.
- Remove the corresponding fuse of the channel to disconnect the transformer
- Modify the software

In principle any channel can be removed. Down to 10 cells, the standard transformer can be used. For a lower number, the transformer design has to be adapted.

Use of 10 Cells

For the use of 10 cells, a software version is already existing. In this case channel 5 and 6 have to be bypassed.

- connect the input terminals between Ch4 and ch6
- remove the fuses R106 and R107

2.6.6 Voltage Overshoot Reduction

The leakage induction is worst at the primary winding. The bigger difference between the number of turns of the primary winding and the secondary ones degrades the coupling. It causes a short voltage overshoot at the primary transistor drain, when the transistor is switched off. The overshoot is limited by the snubber network set up by the components D16, R16 and C16.

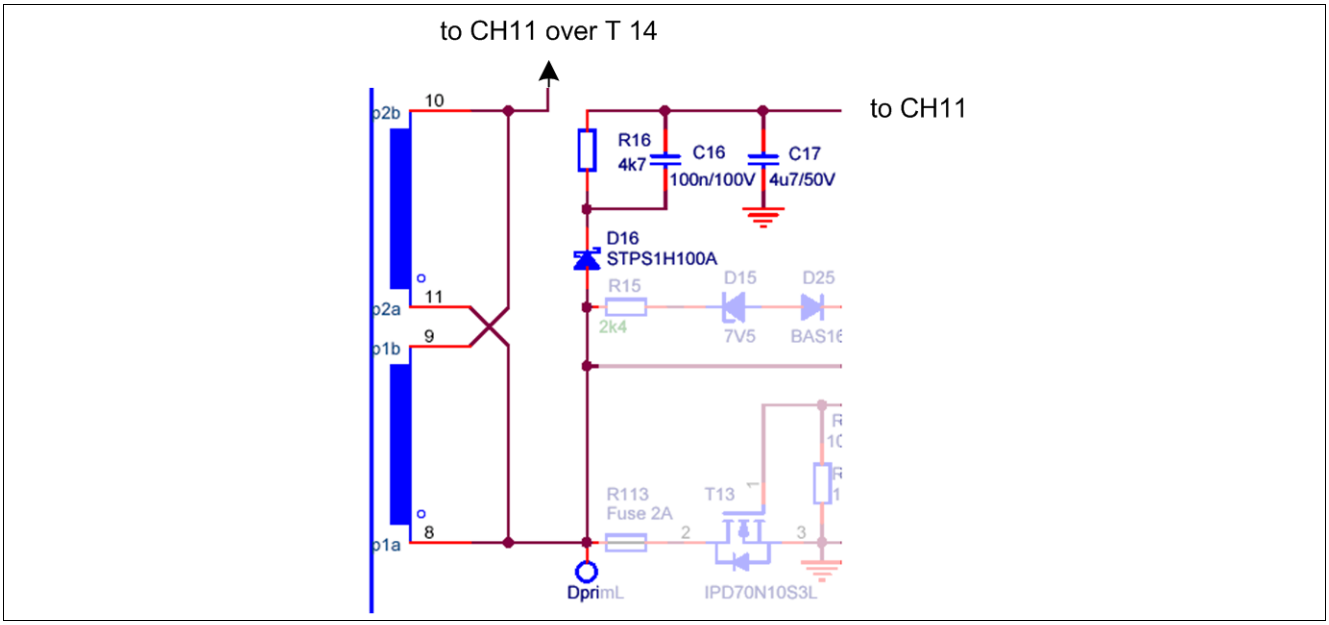

Figure 15 Snubber Network

2.6.7 Degauss Monitoring

The balancing energy is stored in the transformer.To avoid a saturation of the core, a energy transfer into the transformer is only allowed, if it ‘empty’. As shown in Figure 27 and Figure 28 the Drain voltage of the primary MOSFET starts to ring when the current is back to zero level. The below shown filter produces a ‘High’ signal at the degauss monitor pin when the ringing starts. Only with a high level at this port pin, the next pulse is generated.

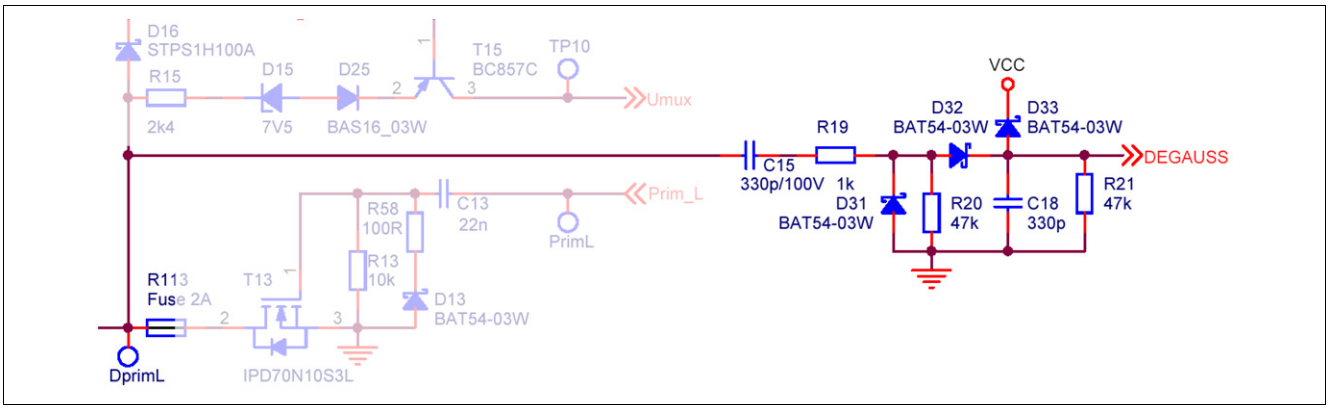

Figure 16 Degauss Monitoring

2.6.8 High Voltage Output for Interblock Balancing

- No interblock balancing:
  If the transistor T14 is switched on, the transformer voltage in the degaussing phase is determined by the block voltage. The voltage in the high voltage winding (pin 30 to pin 25) is lower than the complete string voltage. Therefore no current can flow out of the HV winding.
- Enabled interblock balancing:
  The energy is moved from a single cell out of the block to the complete battery string. For an interblock balancing, T14 is blocked in the degaussing phase.
  The current cannot flow out of the primary winding to the block voltage. The winding voltage in the transformer rises, until a current path over D18 to the complete battery string is opened.

Note: The HV winding of the transformer and the diode type of D18 have to be adapted to the number of blocks in the complete string! Transformer Types are listed in Chapter 3.

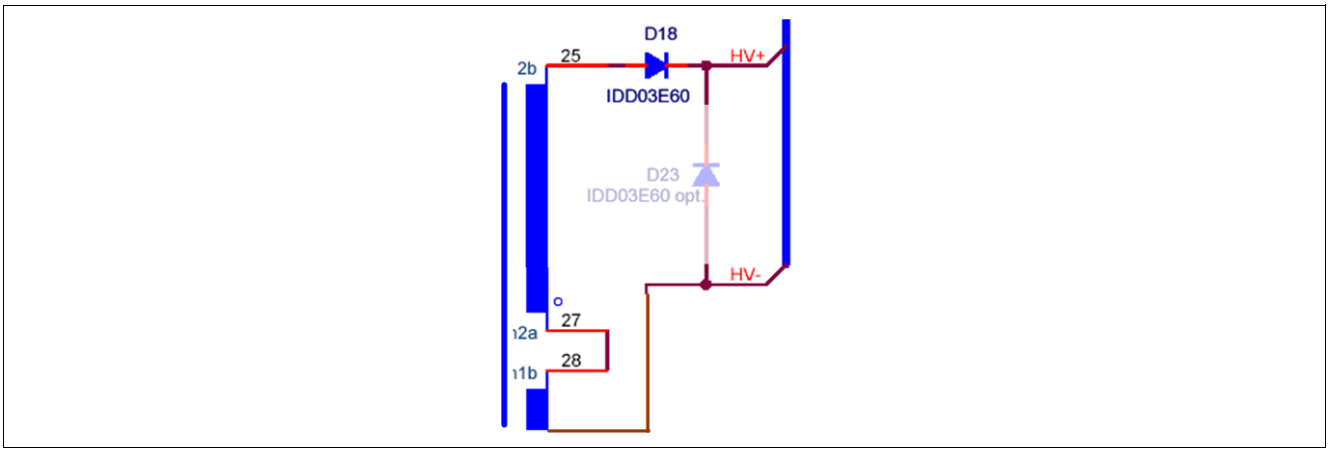

Figure 17 Interblock Output

Interblock Connection

For interblock balancing all HV output terminals have to be connected in parallel to the complete stack Voltage.

For this reason, the HV winding has to be adapted to the number of battery blocks. The corresponding transformer types are listed in **"Transformer Versions" on Page 23**.

Note: The interblock balancing must only be started, if the HV outputs are connected. Otherwise the stored energy in the transformer would lead to an avalanche effect in the PrimH transistor T14.

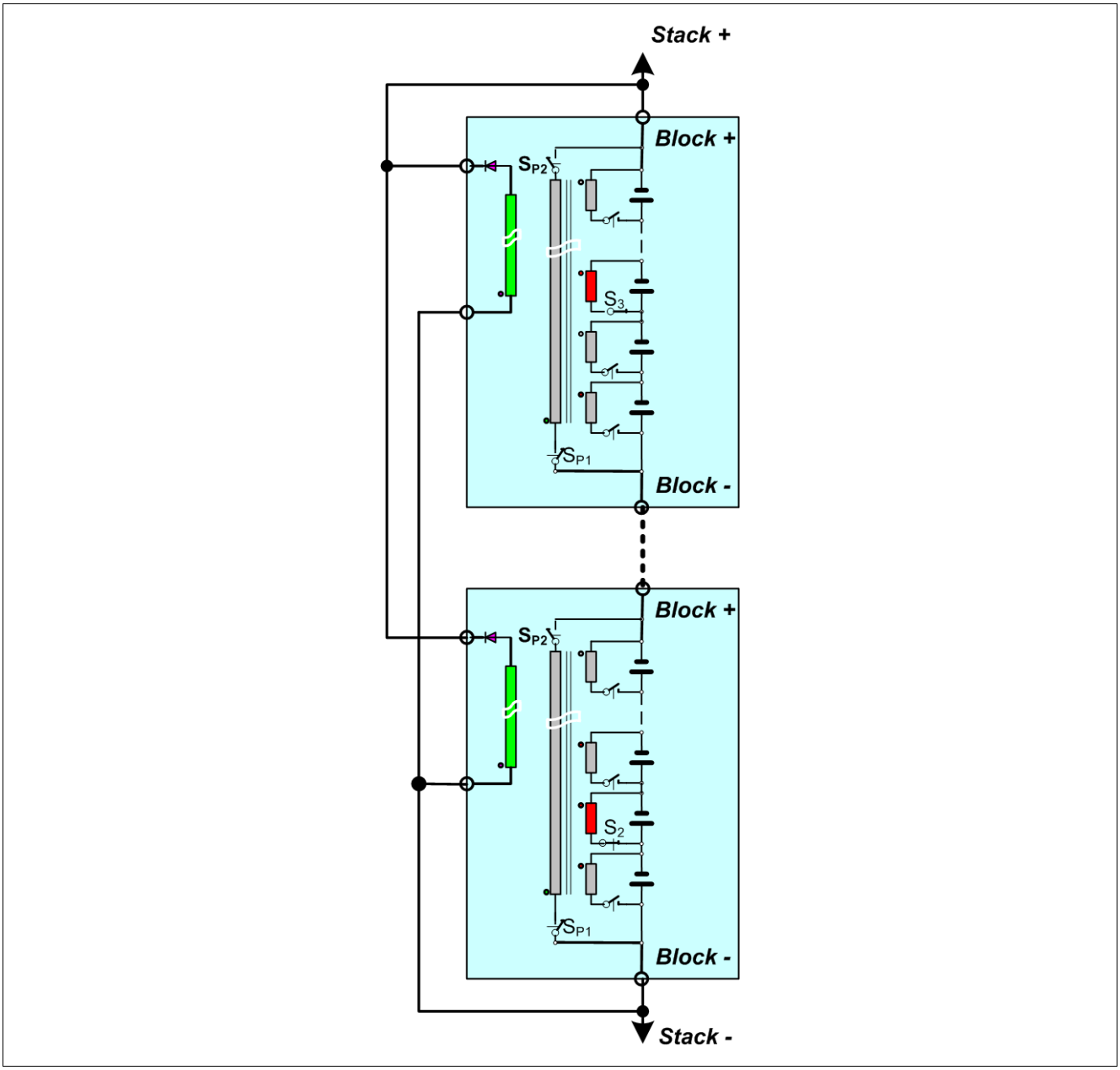

Figure 18 Interblock Connection

2.7 Circuit Diagram Part 1 (Controller)

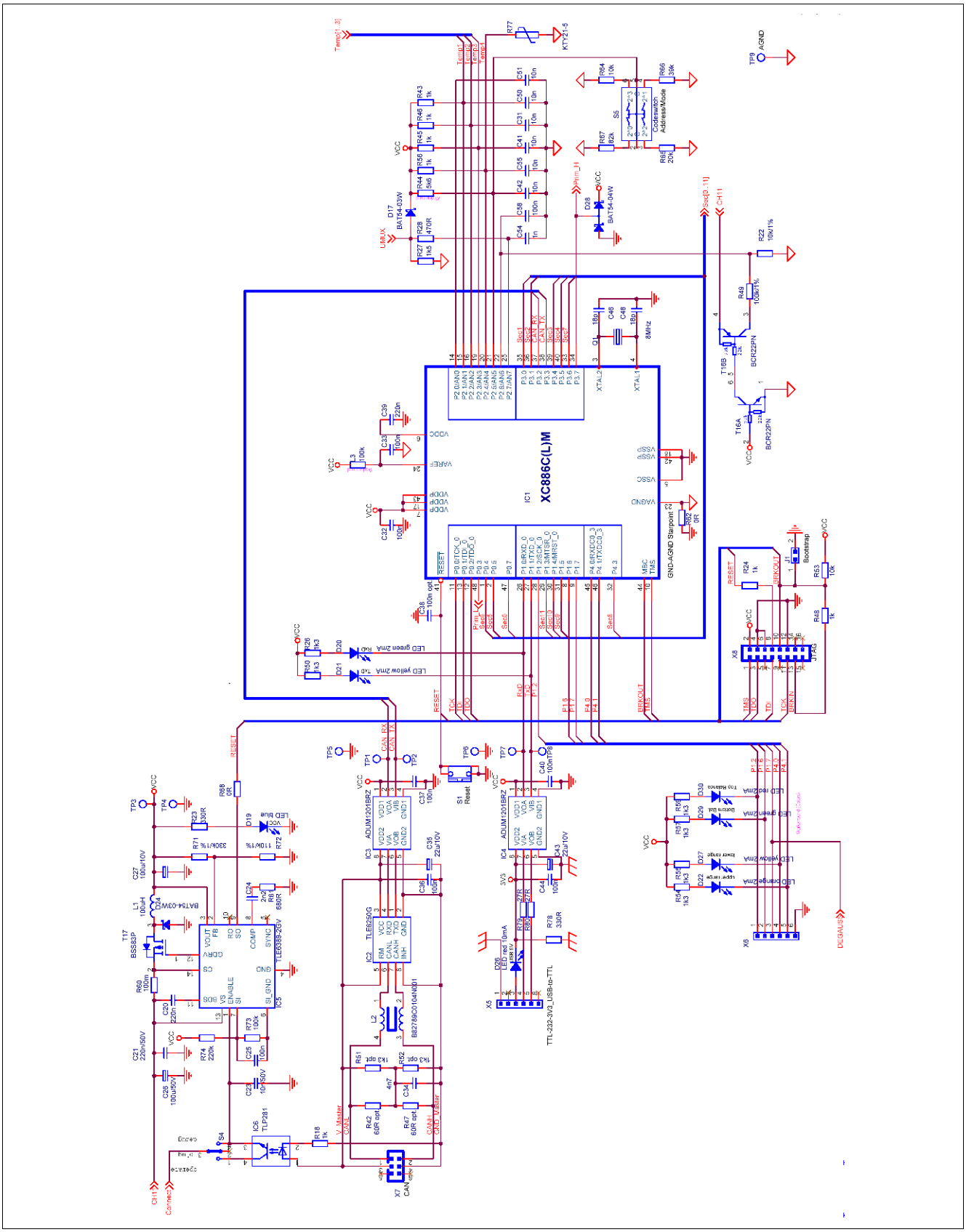

Figure 19 Circuit Diagram Part 1 (Controller)

2.8 Circuit Diagram Part 2 (Power)

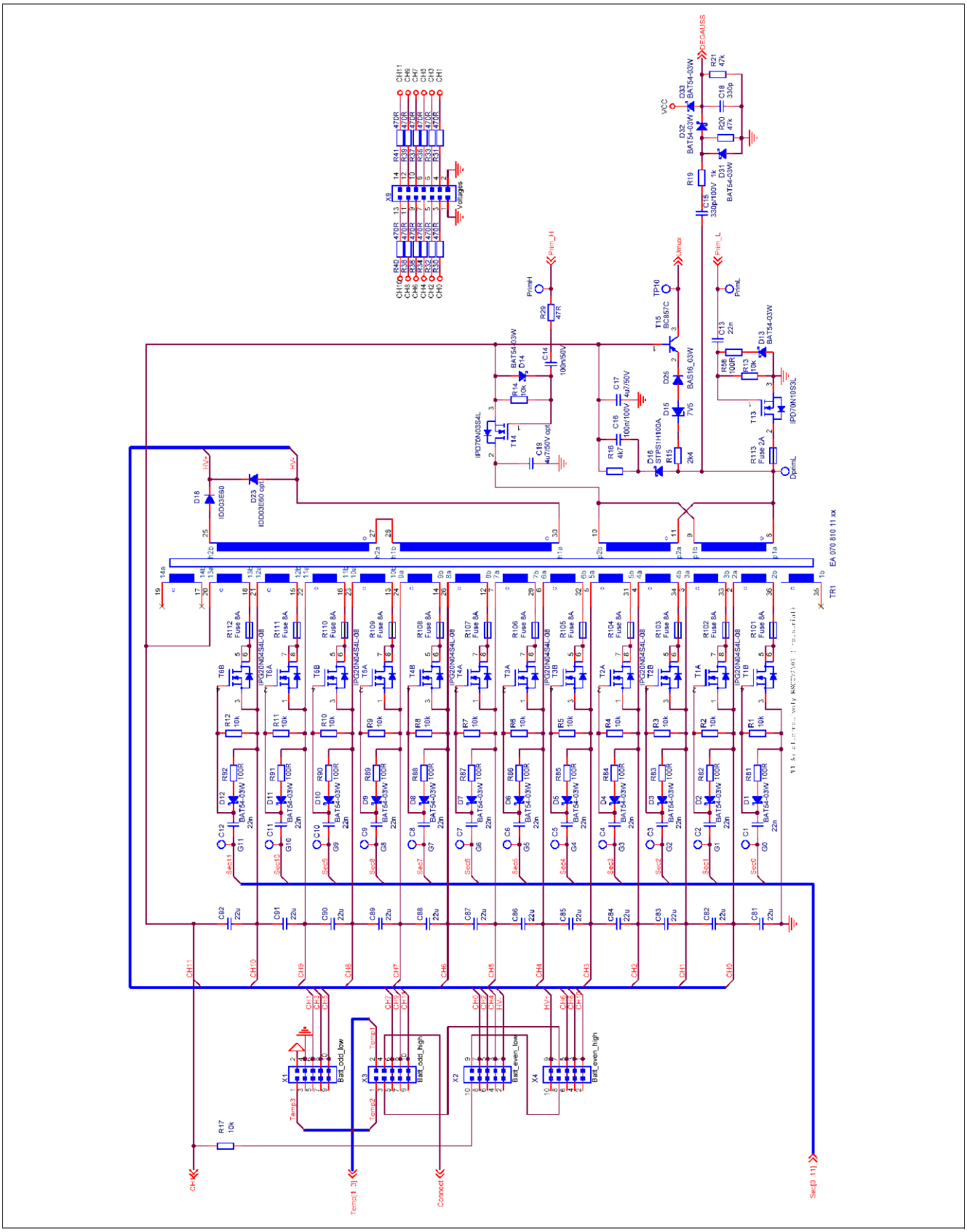

Figure 20 Circuit Diagram Part 2 (Transformer)

2.9 Board Layout

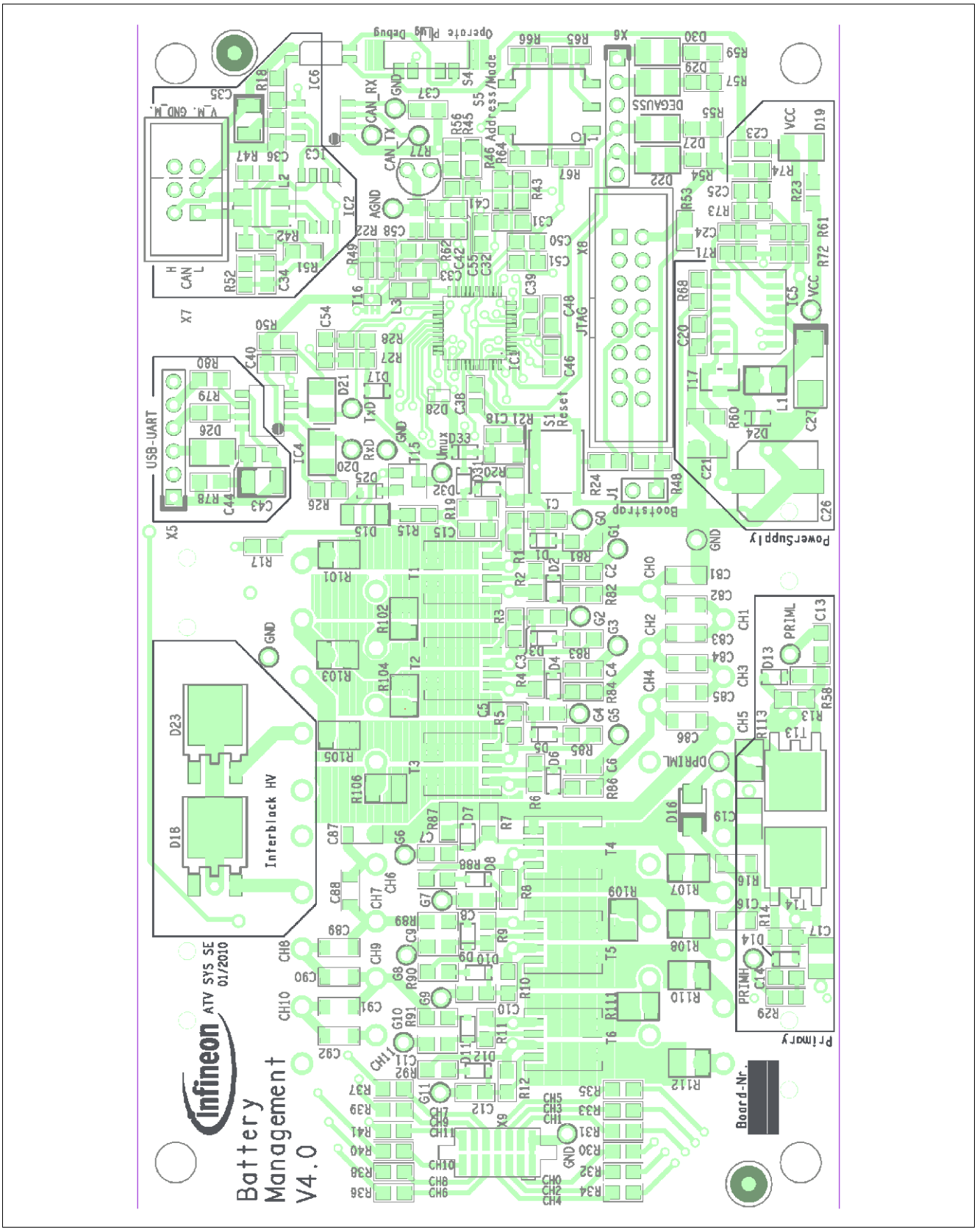

Figure 21 Board Top View

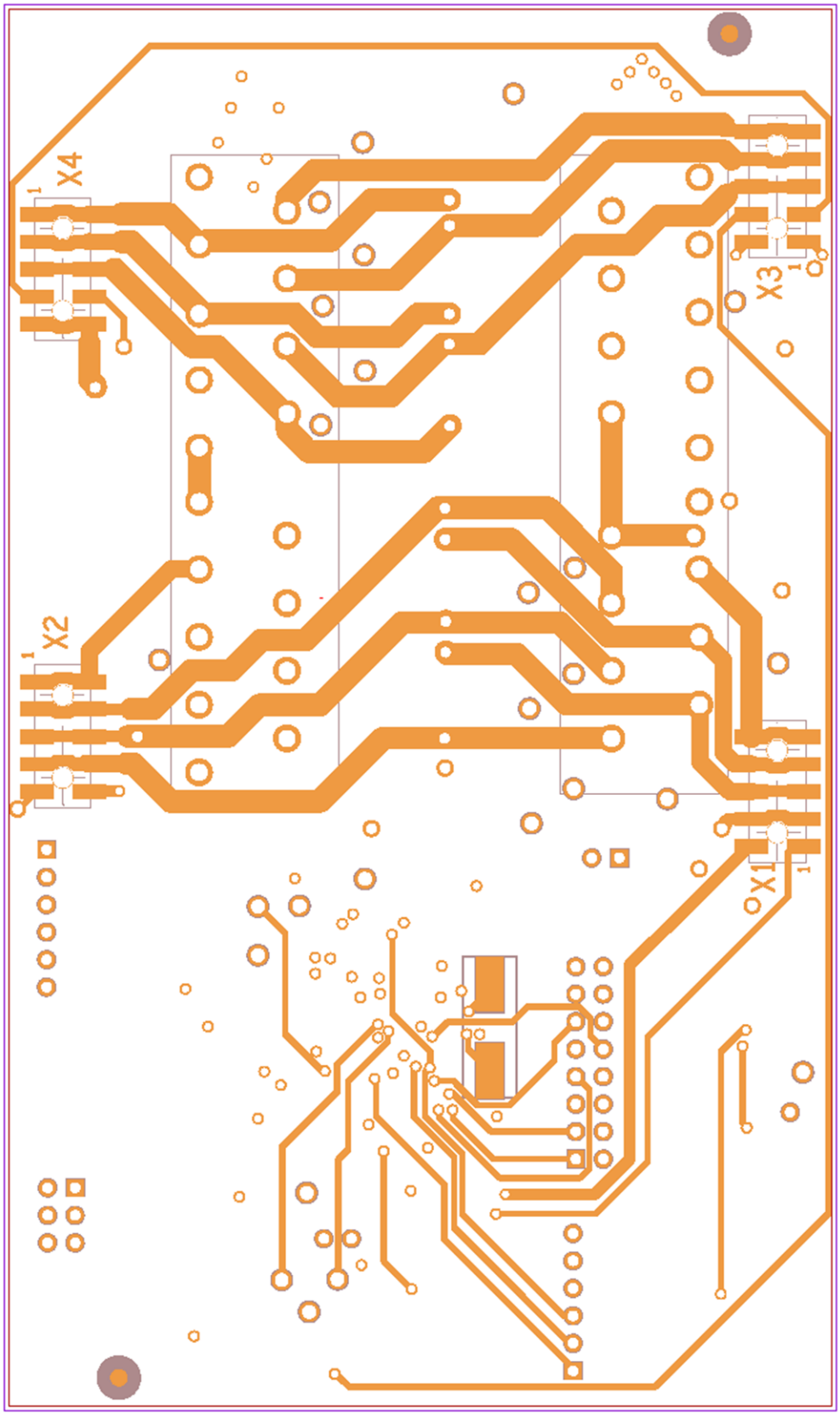

Figure 22 Board Bottom View

3 Transformer Versions

The transformers are manufactured by Vogt electronics (Sumida)

Part Number	Number of Blocks	Primary Inductance [µH]	Remarks
EA 070 810 11 **18**	4	70	In E-Buggy
EA 070 810 11 **19**	2	70	For system test setups
EA 070 810 11 **21**	10	70	In E-Cart with 330V total voltage
EA 070 810 11 **22**	1	70	No HV windings
II 100 224 21 01	1	50	For Super Caps

4 Connection to Battery Cells

Note: The energy in battery cells is enormous. The smallest handling error may lead to short-circuit currents of 1000 Amps or even more. A careful handling of battery setups is strictly mandatory.

To connect battery cells to the board, it is recommended to use a pluggable solution. In this case, the cells can be linked to an adapter before they get in touch with the board electronics. If any reworks are done on the board, it has to be removed from the connector.

Adapter Board

The four connectors X1 to X4 fit to the 'Minimate' series of Samtec, type IPS1-105-01-S-D. These connectors are available as through-hole or SMD version. They are arranged in a 0.1 inch raster.

For a rapid and easy connection, an adapter board is available. Using the 4mm jacks, all cell can be individually charged or discharged.

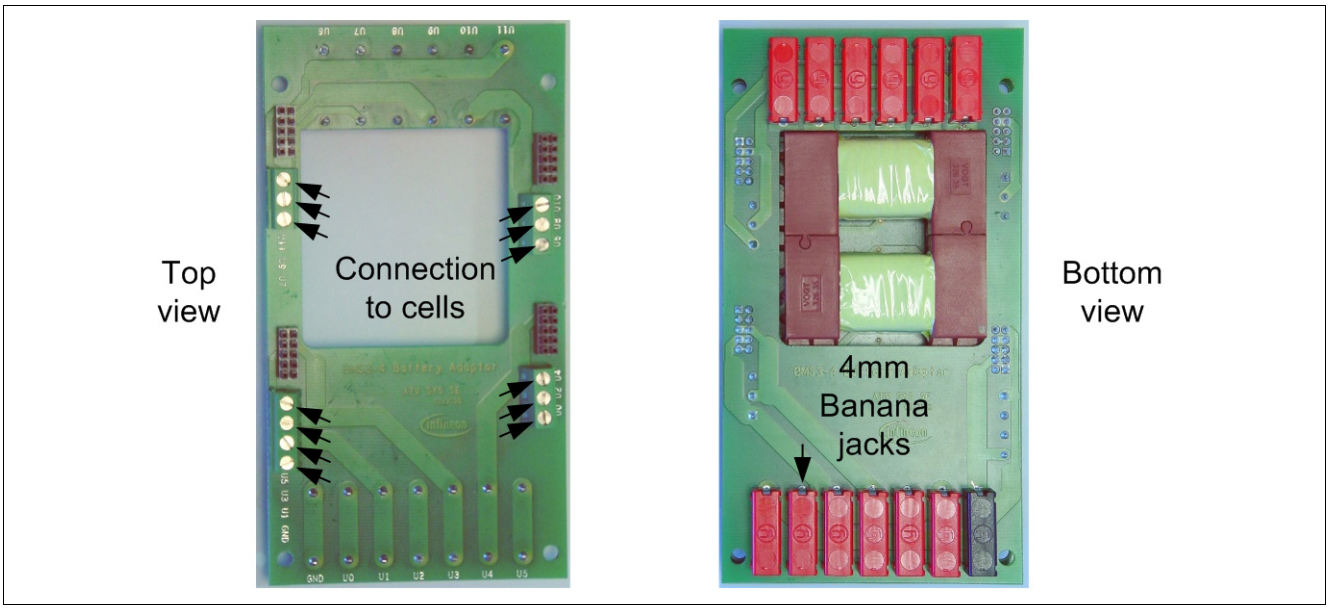

Figure 23 Adapter Board

Wiring Example of a Battery Block

The wires between the cell nodes and the board should have at least 1mm². Also the length should be as small as possible in order to avoid voltage overshooting caused by parasitic inductances. The balancing peak current rise up to 20 Amps. Tolerable values are up to 30cm. At least the ground connection should be as short and low-ohmic as possible.

The following example shows a block with 12 cell of the type ANR26650 from A123. Ten fresh cells with a green body are combined with two older samples.

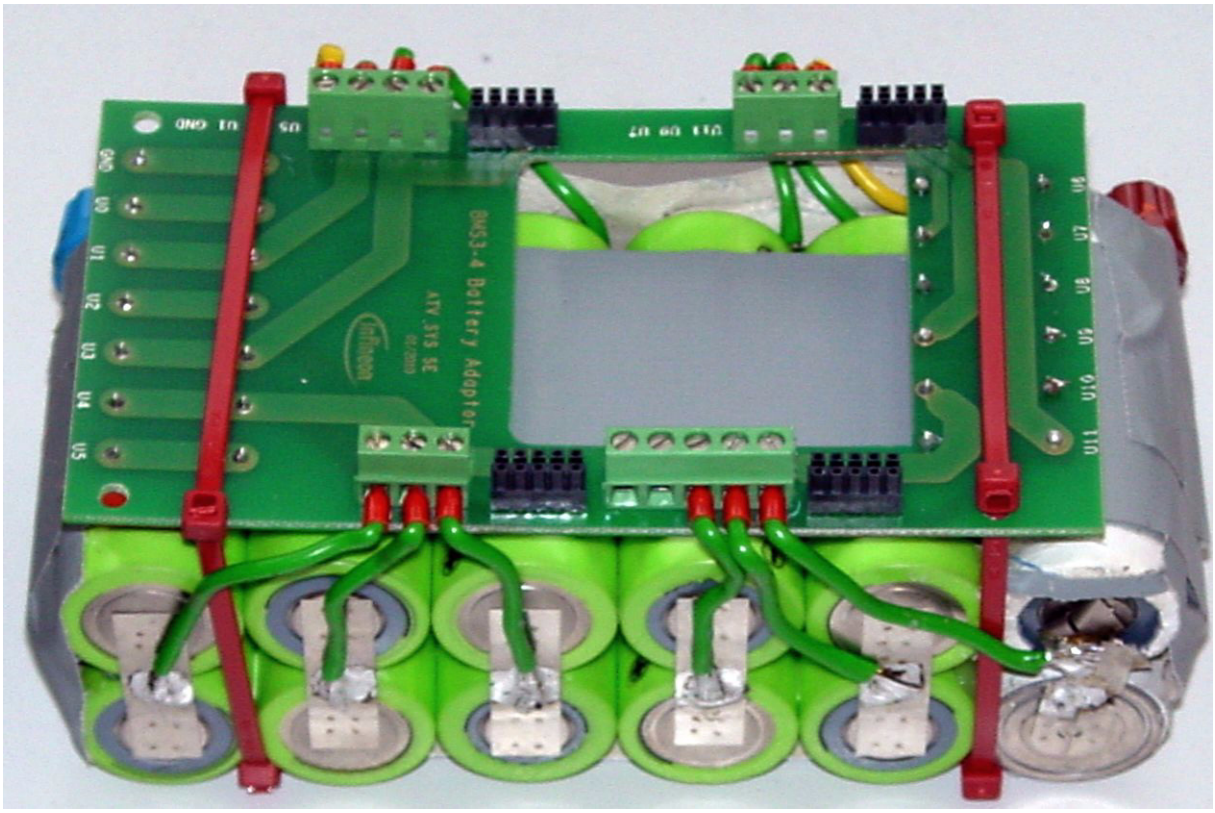

Figure 24 Wiring Example

5 PCB Modifications

5.1 Version for Super Caps (double layer caps)

In principle, the balancing of caps is similar to battery cells. One difference between these two storage elements is the voltage range. Voltages down to zero for caps is within the normal range. Only voltages over the limit may create damages. Therefor it makes sense to extend the operational range to lower voltages.

5.1.1 Different transfer function for the Voltage Scan

1. To extend the measurement range to lower voltages, the offset zener diode D15 has to be replaced by a normal silicon diode.
2. For an increased gain value, R15 has to be modified.

The exact component values are listed in **“Component Values for different Board Versions” on Page 13**

5.1.2 Degauss circuit

For a wider operation range with caps, the degauss monitor circuit should be modified.

- remove R 20
- remove R 21
- Change C 18 to 100pF

6 Operational Waveforms

The following pictures are made under following conditions:

- Block with 12 cells Litec 40Ah
- State of charge: ~97% (voltage 4.15V)

Note: All timings are generated by the µController. Therefore they depend on the flashed software version.

6.1 Voltage Scan

A scan interval consists of one scan pulse for each cell voltage plus one dummy pulse in front. This additional pulse is used to 'preheat' the system, so that all scan pulses have the same history.

The pulses are generated in reverse order starting with the cell with the highest voltage level (U11 in case of 12 cells). The last pulse is related to U0.

All cell voltages are measured within a time interval of about 580µs.

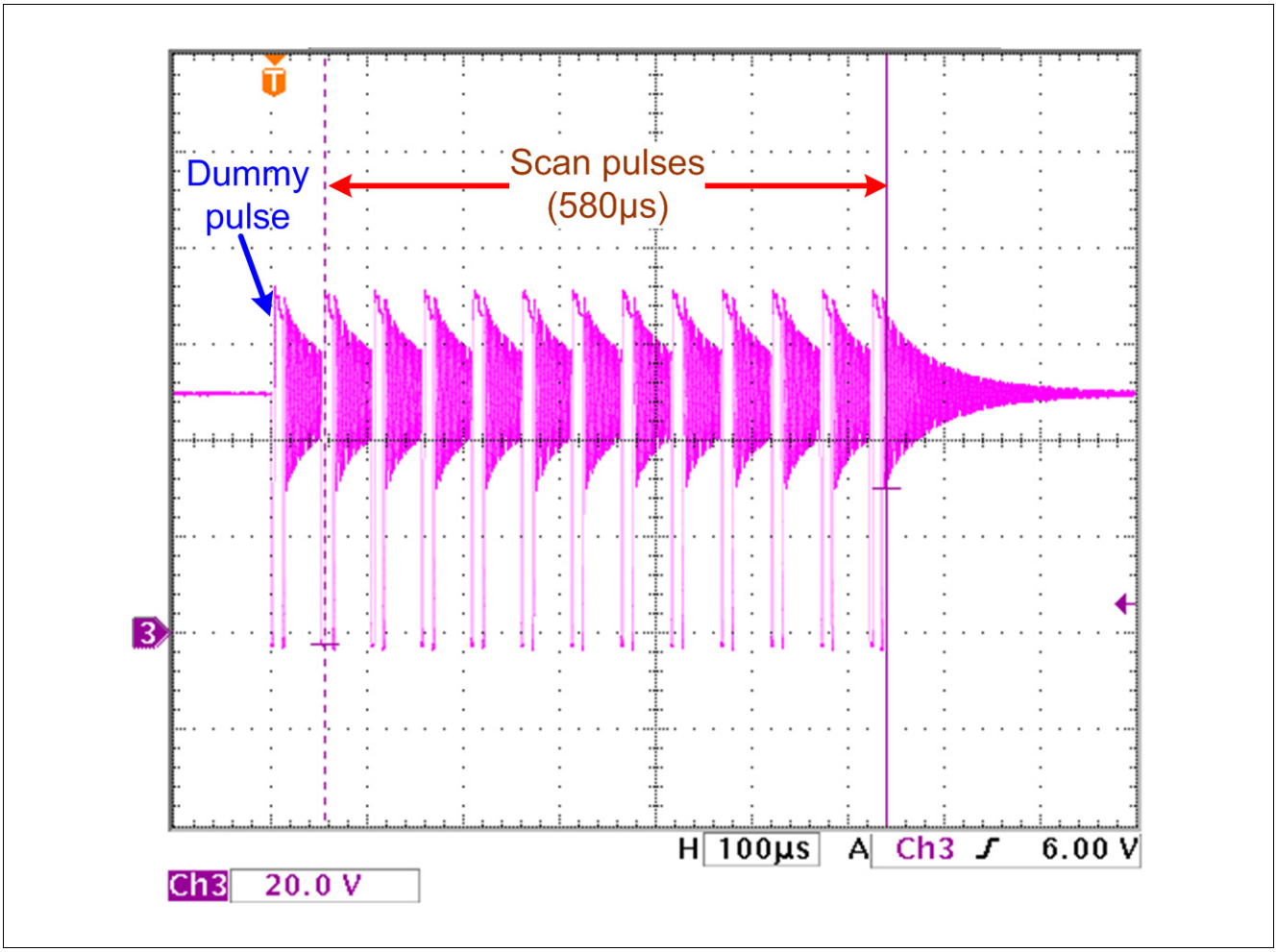

Figure 25 Complete Voltage Scan (Measurement point: Drain of primary MOSFET)

6.2 Single Scan Pulse

Figure 26 shows the pulse sequence of a single cell voltage scan pulse. This timing was optimized after a many investigations.

The sequence in detail:

1. **Primary MOSFET on:** Precharge the transformer
2. **All MOSFETs off:** discharge over all reverse diodes of the secondary MOSFETs in parallel. The voltage in the low pass filter of the scan path is stabilized.
3. **The selected secondary MOSFET is switched on:** The remaining magnetic energy in the transformer is directed into the selected cell. The voltage in a transformer winding turn is now proportional to the selected cell voltage. Shortly after the zero crossing of the transformer, the voltage at the Umux is sampled. This allows the voltage measurement nearly independent on the ohmic resistance in the measurement path (Connector, copper resistance of the transformer, R_{DSon}.). The ADC is triggered shortly, before the secondary transistor is switched off.

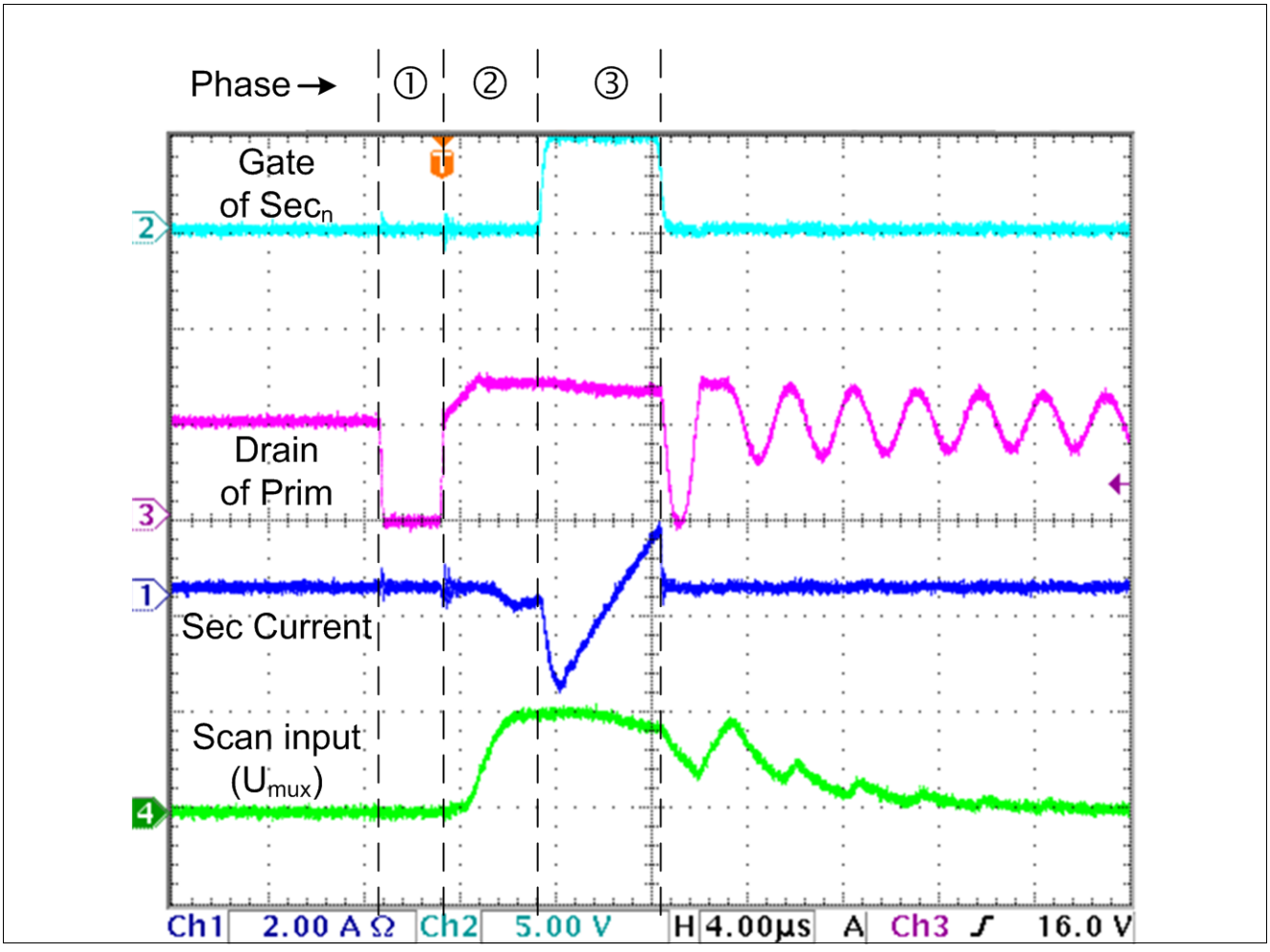

Figure 26 Voltage Scan Zoom to single Value

6.3 Bottom Balancing Pulse

The Bottom balance mode is used to support weak cells. Their voltage level is lower than the average cell voltage of the block.

One pulse sequence consists of two phases:

1. **Primary Phase:** The primary MOSFET is on. The Drain voltage is zero and the current rises linearly. The di/dt depends on the primary inductance and the block voltage. The peak current value can be determined by the on-time of the primary MOSFET.
2. **Secondary Phase:** The selected secondary MOSFET is on. The transformer work as current source until the energy content of the transformer is relieved. Without direct current measurement, it is not possible to detect this situation. Therefore it is useful to switch off the transistor before the current is zero. The remaining current flows over the integrated reverse diode. This can be seen as a small voltage increase at the primary Drain voltage.

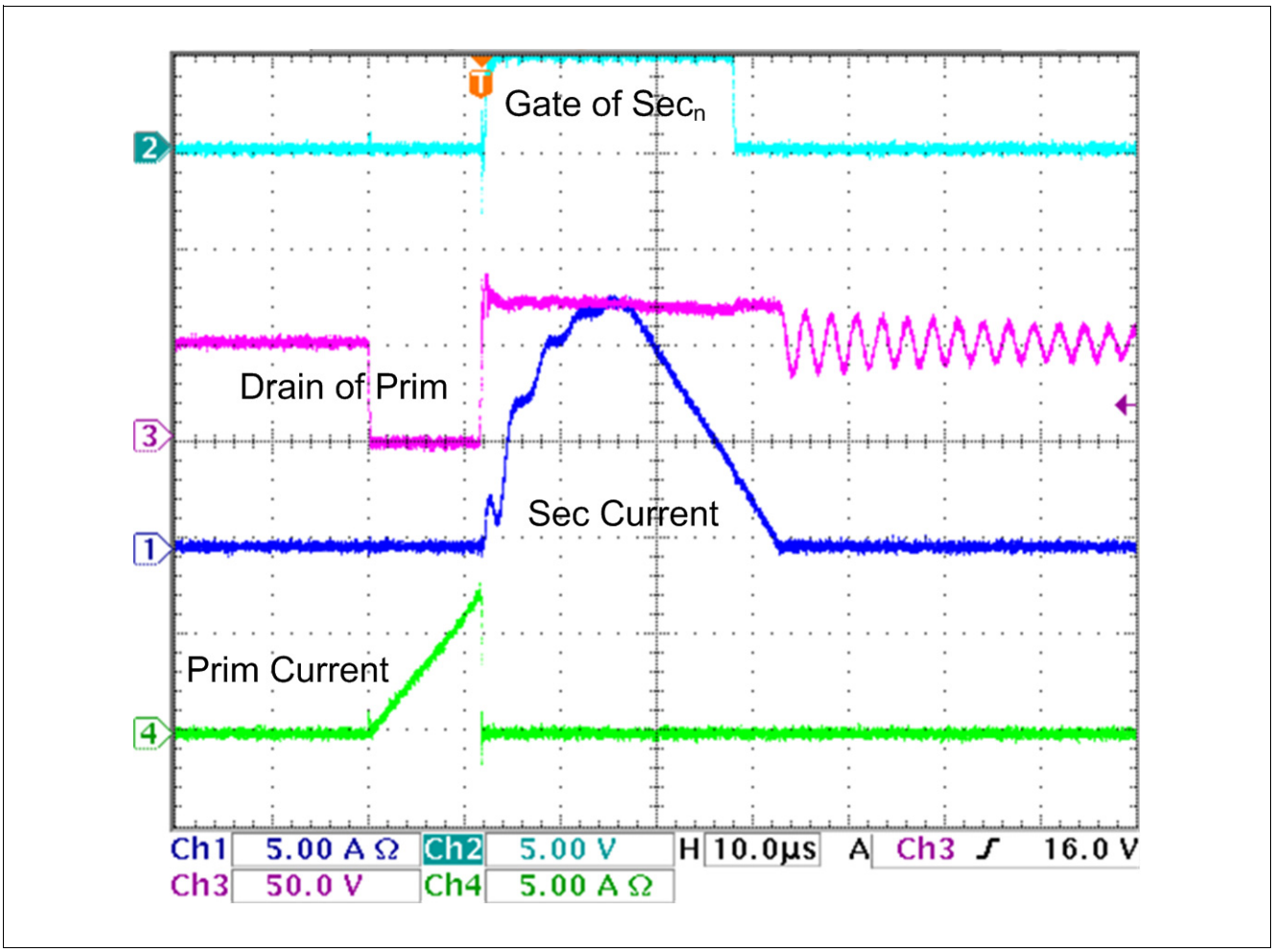

Figure 27 Bottom Balancing, Single pulse

6.4 Top Balancing

6.4.1 Single Top Balancing Pulse

The Top balance mode is used in the charge phase of the battery cells. In order to avoid an overcharge of strong cells, the cell with the highest voltage has to be discharged.

Energy is moved from a single cell into the transformer. Then the energy portion is distributed over the primary winding to all cells in the block.

The timing sequence is inverse to the Bottom balance mode.

One pulse sequence consists of two phases:

1. **Secondary Phase:** The selected secondary MOSFET is on. The secondary current rises linearly. The voltage at the primary Drain increases additionally to the block voltage. The di/dt depends on the secondary inductance and the selected cell voltage. The current peak at the beginning is caused by parasitic capacities.
2. **Primary Phase:** The primary MOSFET is on. The transformer work as current source until the energy content of the transformer is relieved. Like in the Bottom balancing mode, the complete degaussing cannot be measured.Therfore it is useful to switch off the transistor before the current is zero. The remaining current flows over the integrated reverse diode.

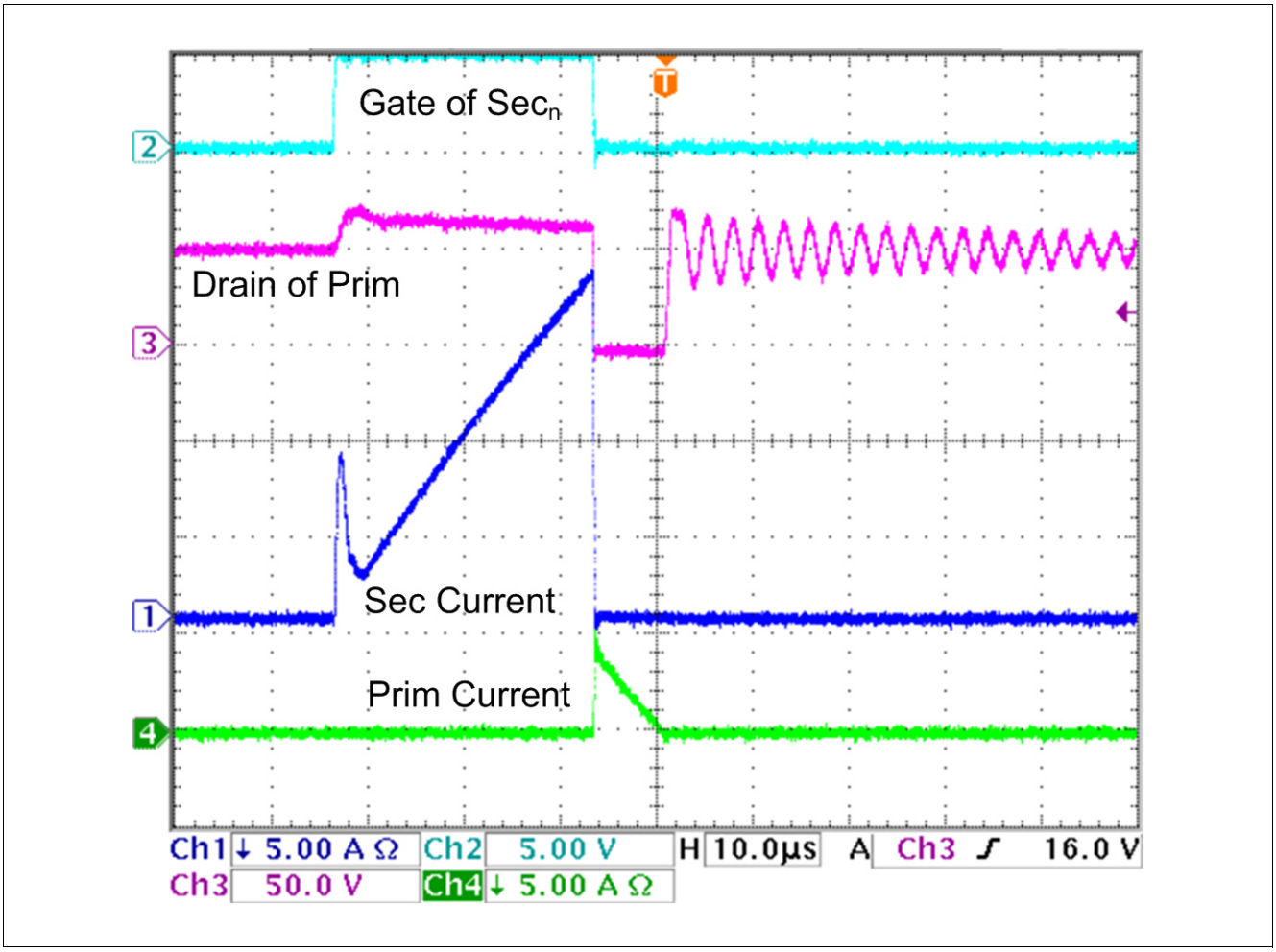

Figure 28 Top Balancing, Single Pulse

6.5 Pulse Sequences (Screenshots)

The following screenshot show the waveform from a board connected to 12 cells from A123. The cells were charged to the nominal voltage of 3.3V.

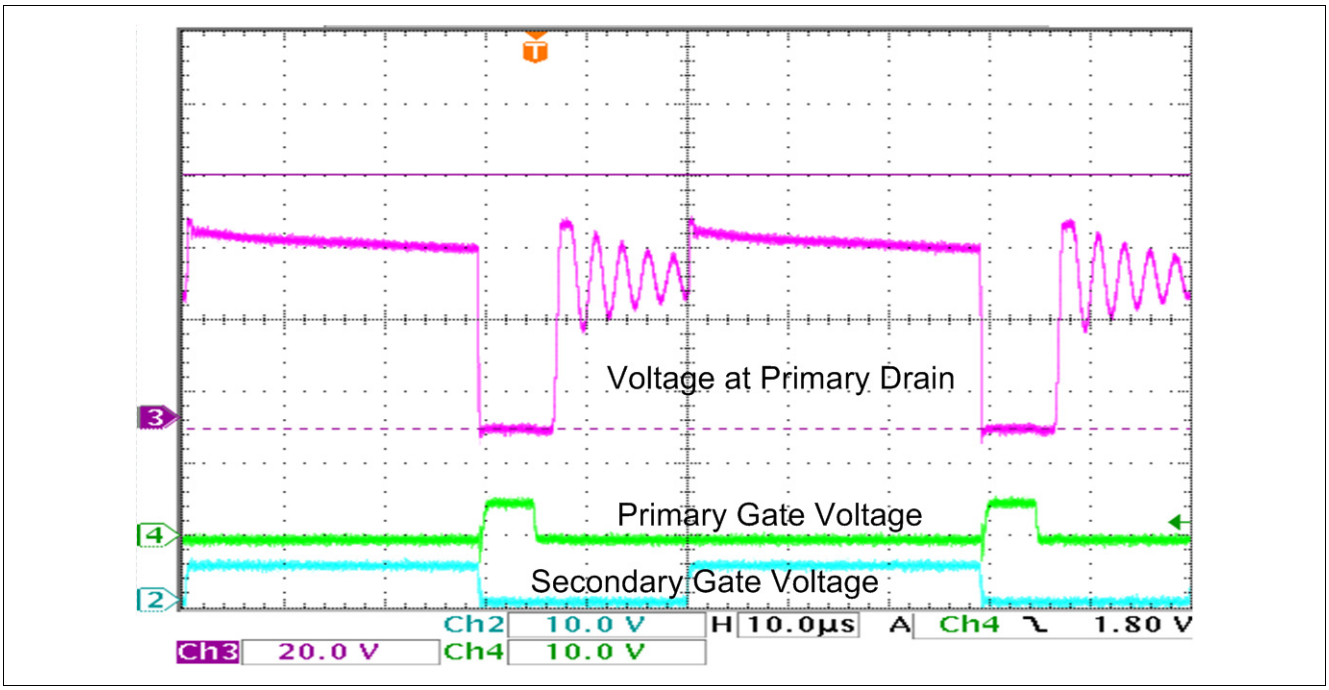

Figure 29 Top Balancing Sequence

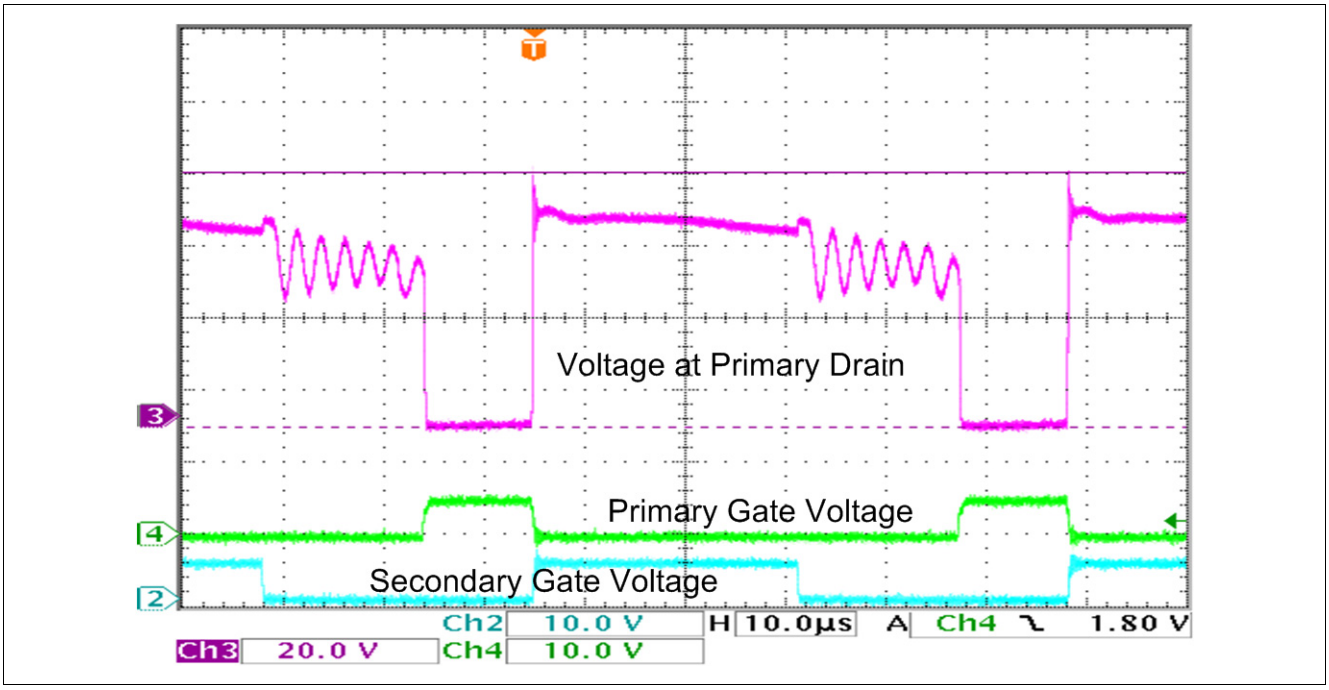

Figure 30 Bottom Balancing Sequence

7 Initial Test and Calibration Procedure

This procedure has to be done with new boards. It is also recommended after repair works or a strange behaviour of the board.

- **Optical inspection**

Have an intensive look to all components for

  - damages
  - bad solder spots
  - short circuits

- **Check the number of supported cells**

If the cell block has only 10 cells, the fuses R106 and R107 have to be removed

- **Set the power switch S4 to position ‘Plug’**
- **Plug the board on a battery stack**

Note: In case of short circuits, big currents could flow. Be prepared to disconnect the board immediately.

- **Set the power switch to position ‘Debug’**

The blue LED should be on

- **Measure the V_{CC} voltage at the test point near R72**

The value has to be between 5V and 5.5V

- **Flash the suitable software following the instructions in chapter “Software Update” on Page 11**
- **Set the rotary switch to position ‘0’.**
- **Open a terminal program like ‘Teraterm’**
- **Press the ‘*Reset* key’**

A welcome message appears. It shows the version (number of cells, board version, compiling date) and the stored calibration data.

- **Start the self test by pressing the key ‘D’**

In this test only very small pulses are applied to the transformer. The measurement results on the U_{MUX} input (P1.7) are printed (in ADC digits). The test are:

  - Secondary channels: A pulse can be only measured, if following conditions are fulfilled: the Mosfets work , the fuses are not blown and a cell voltage is applied (tip: measure the DC voltage at both side of the fuses)
  - Primary transistor (PrimL): A pulse can be measured, if the Mosfet T13 works and is controlled by a Gate signal > 3.5V, the fuse R113 is not blown and the block voltage is applied to the Drain (tip: measure the DC voltage at both side of fuse R113)
  - Primary transistor high side for interblock balancing control (T14): This test shows, if the transistor is working. The difference between the measured level values has to be at least 100 digits. If the PrimL test is passed and the PrimH test fails, the transistor is replaced or short circuited. The board works, but interblock balancing cannot be performed.

- **Waveform check**

Connect an oscilloscope probe to the test point at the Drain of T13 (marked *DPRIML*). Use the terminal program and send e.g. ‘T1’. A single Top balancing pulse is generated. Then generate a single Bottom balancing pulse with the message ‘B1’. Compare the waveform with the pictures on Page 29 and Page 30. This bottom balancing test shows any faults in the snubber network. In case of an error the voltage peak is too high.

- **Calibration of the voltage measurement**.

First measure all cell voltages and the block voltage and note the values. They are avilable at the measurement adapter X9 (see chapter **"Diagnosis and Calibration Connector" on Page 10**).

There are two way to enter the values:

– Step by step: Send a 'C' and follow the instuctions. The values have to be entered with 4 digits (e.g. 3.654).
– In a string: Type into an Excel sheet a string like following example:

	U0	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U_Block	
12 cells	3.297	3.297	3.296	3.297	3.297	3.333	3.234	3.297	3.298	3.297	3.297	3.296	32.974	a
10 cells	3.297	3.297	3.296	3.297	3.297	3.297	3.298	3.297	3.297	3.296	32.974	a		

Copy the green or yellow marked cells to the clipboard.
Then send 'A' from he terminal program.
Paste the string into the terminal window by using the right mouse button.
Confirm with 'Y'.

After the calibration send 'S' in order to generate a voltage scan. Compare the values in the terminal window with the real measured values.

- **Now start the balancing routine** by sending 'U'.

Note: The best calibration results can be reached, if all cell voltages are close together. If the cells are disbalanced, work in more steps. Make a first calibration and start the balancing routine. When the voltage difference is <10mV, make a new calibration.

8 Bill of Material

Item	Qty	Part#	Name	Category
1	1	D25		Diode
2	19	D1,D2,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,D17,D24,D31,D32,D33	BAT54-03W	Diode
3	1	D17	BAT54-03W	Diode
4	1	D28	BAT54-04W	Diode
5	1	D18	IDD03E60	Diode
6	1	D23	IDD03E60 opt.	Diode
7	1	D16	STPS1H100A	Diode
8	2	IC3,IC4	ADUM1201BRZ	IC
9	1	IC2	TLE6250G	IC
10	1	IC5	TLE6389-2GV	IC
11	1	IC1	XC886C(L)M	IC
12	1	L1	100uH	Inductor
13	1	L2	B82789C0104N001	Inductor
14	1	L3	MI0805K400R-10 100k	Inductor Wid.
15	8	C25,C32,C33,C36,C37,C40,C44,C58	100n	Capacitor
16	1	C38	100n opt.	Capacitor
17	1	C16	100n/100V	Capacitor
18	1	C14	100n/50V	Capacitor
19	1	C27	100u/10V	Capacitor
20	1	C26	100u/50V	Capacitor
21	6	C31,C41,C42,C50,C51,C55	10n	Capacitor
22	1	C23	10n/50V	Capacitor
23	2	C46,C48	18p	Capacitor
24	1	C54	1n	Capacitor
25	2	C20,C39	220n	Capacitor
26	1	C21	220n/50V	Capacitor
27	13	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13	22n	Capacitor
28	12	C81,C82,C83,C84,C85,C86,C87,C88,C89,C90,C91,C92	22u	Capacitor
29	2	C35,C43	22u/10V	Capacitor
30	1	C24	2n2	Capacitor
31	1	C18	330p	Capacitor
32	1	C15	330p/100V	Capacitor
33	1	C34	4n7	Capacitor
34	1	C17	4u7/50V	Capacitor
35	1	C19	4u7/50V opt.	Capacitor
36	1	D19	LED blue 10mA	LED
37	2	D20,D29	LED green 2mA	LED
38	1	D22	LED orange 2mA	LED
39	1	D26	LED red 10mA	LED
40	2	D21, D27	LED yellow 2mA	LED
41	1	IC6	TLP281	Opto coupler
42	1	Q1	8MHz	Quartz
43	1	S5	Codesw itch	Sw itch
44	1	S4	SlideSw itch_4pol	Sw itch

Item	Qty	Part#	Name	Category
45	1	S1	SW_Bu12G1725	Switch
46	1	R113	Fuse 5A Littelfuse Serie 451	Fuse
47	12	R101,R102,R103,R104,R105,R106,R107,R108,R109,R110,R111,R112	Fuse10A Littelfuse Serie 451	Fuse
48	1	X7	DIL_2x3_wanne	Connector
49	1	X8	DIL_2x8_wanne	Connector
50	1	J1	Jumper	Connector
51	4	X1,X2,X3,X4	Samtec IPT1-105-01-S-D-VS-A	Connector
52	1	X9	Samtec_SFM-107-L2-S-D-LC	Connector
53	2	X5,X6	SIL_1x6	Connector
54	1	R77	KTY21-6/KTY81-110	Temp.Sensor
55	1	TR1	Transformer_Vogt_U44_36-1pin / W9	Transformer
56	1	T15	BC857C	Transistor
57	1	T16	BCR22PN	Transistor
58	6	T1,T2,T3,T4,T5,T6	IPG20N04S4L-08 (autom.) or BSC072N03 (ind.)	Transistor
59	1	T17	BSS83P	Transistor
60	1	T14	IPD70N03S4L	Transistor
61	1	T13	IPD70N10S3L	Transistor
62	2	R62,R68	0R	Resistor
63	1	R73	100k	Resistor
64	1	R49	100k/1%	Resistor
65	1	R60	100m (MilliOhm)	Resistor
66	13	R58,R81,R82,R83,R84,R85,R86,R87,R88,R89,R90,R91,R92	100R	Resistor
67	17	R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12,R13,R14,R17,R53,R64	10k	Resistor
68	1	R22	10k/1%	Resistor
69	1	R72	110k/1%	Resistor
70	7	R18,R24,R43,R45,R46,R48,R56	1k	Resistor
71	1	R19	1k	Resistor
72	6	R26,R50,R54,R55,R57,R59	1k3	Resistor
73	2	R51,R52	1k3 opt.	Resistor
74	1	R27	1k5	Resistor
75	1	R65	20k	Resistor
76	1	R74	220k	Resistor
77	2	R79,R80	27R	Resistor
78	1	R15	2k4	Resistor
79	1	R71	330k/1%	Resistor
80	2	R23, R78	330R	Resistor
81	1	R66	39k	Resistor
82	13	R28,R30,R31,R32,R33,R34,R35,R36,R37,R38,R39,R40,R41	470R	Resistor
83	2	R20,R21	47k	Resistor
84	1	R29	47R	Resistor
85	1	R16	4k7	Resistor
86	2	R42,R47	60R opt.	Resistor
87	1	R61	680R	Resistor

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